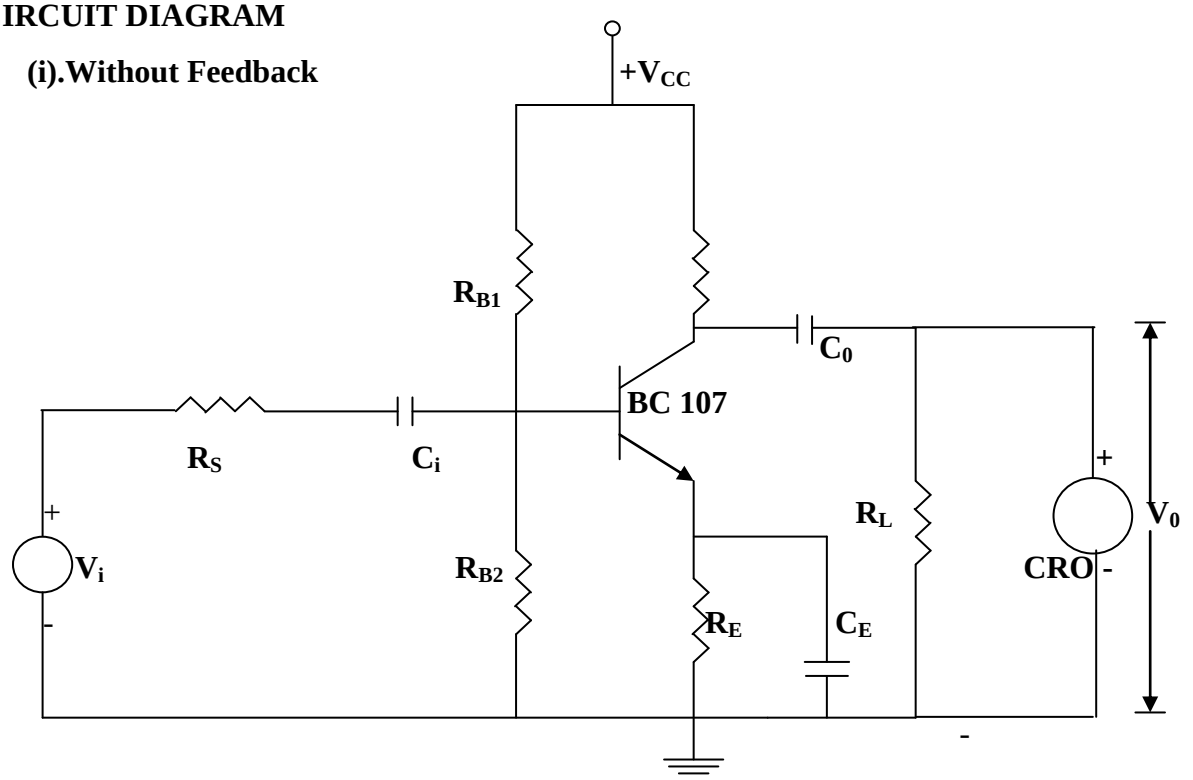
DESIGN AND ANALYSIS

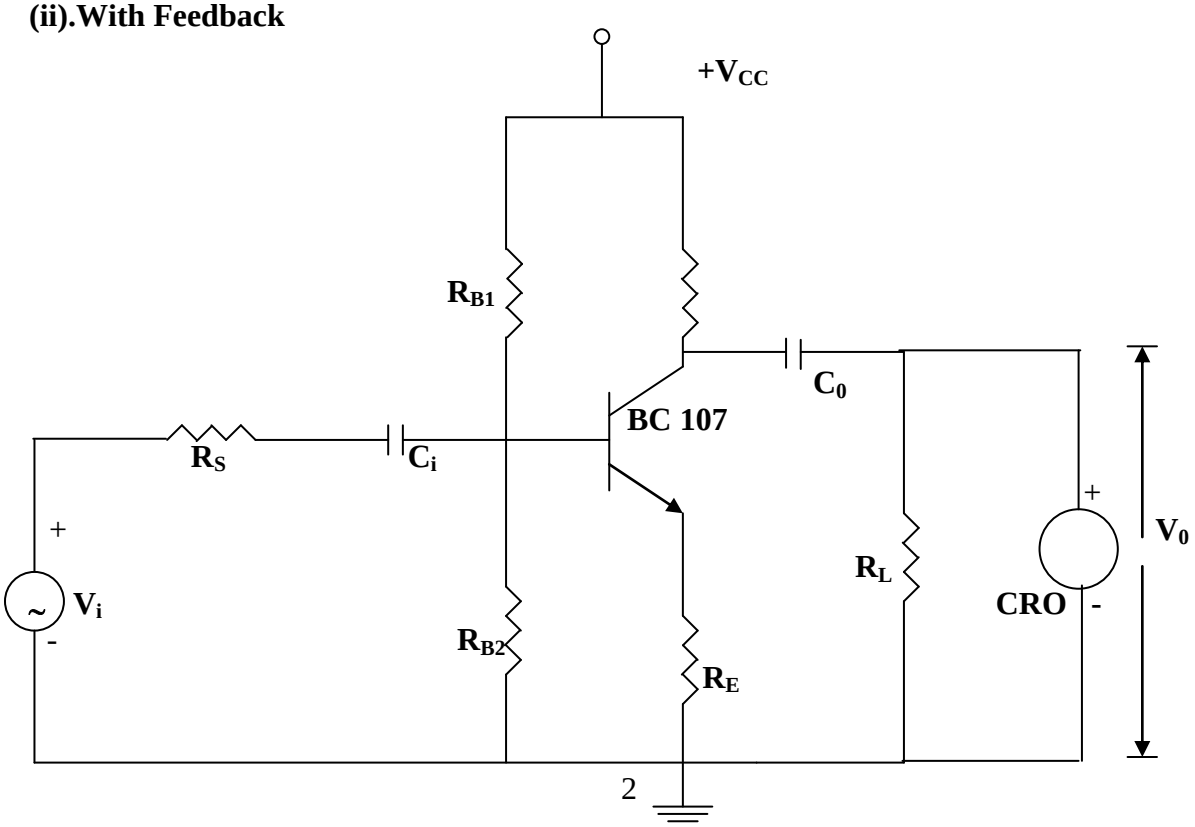
CURRENT SERIES FEEDBACK AMPLIFIER

CIRCUIT DIAGRAM

(i).Without Feedback



(ii).With Feedback



Ex. No.: 1 (a) **CURRENT SERIES FEEDBACK AMPLIFIERS**

Aim:

To design and test the current series feedback amplifier and to calculate the following parameters with and without feedback.

i. Mid-band gain

ii. Bandwidth and cut off frequencies

iii. Input and output impedance.

Apparatus &Components Required:

Sl.No.	Equipments & Components	Range	Quantity
1.	CRO	(0-30) MHz	1
2.	Signal Generator	(0-1) MHz	1
3.	Power Supply	(0-30) V	1
4.	Transistor	BC 107	1
5.	Capacitor	1μF, 0.5μF,	Each 2
6.	Resistor	1K, 10KΩ, 470Ω, 33KΩ	Each 1

Theory:

To construct an amplifier with precise gain we must employ negative feedback techniques. This makes the gain to be independent of β and dependent only on the characteristics of the feedback network. Usually resistors are used to construct feedback networks. When high input and output impedance and finite gain are required, Current series feedback is employed. The circuit diagram shows a current series amplifier. It can be seen that a current series feedback amplifier results in, when the emitter bypass capacitor of the common emitter amplifier is removed.

Making $i_o = 0$ (output opened), feedback signal becomes zero. So sampling is done for current. Making $V_o = 0$, the feedback signal does not become zero. In current series circuit source voltage (V_s) and feedback voltage are in series. So mixing is series. In current series input resistance R_i increases, output resistance R_o also increases**.**

Tabulation:

(i). Without Feedback

Frequency (Hz)	Output Voltage (V)	Gain = 20 log(Vo/Vin) (dB)

(ii).With Feedback

Frequency (Hz)	Output Voltage (V)	Gain = 20 log(Vo/Vin) (dB)

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set input voltage V_i = 50mV, 1Khz using signal generator.
3. Keeping the input voltage constant, vary the frequency from 0Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: Gain (dB) Vs Frequency (Hz).
5. Find the input and output impedance.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
8. Remove emitter capacitor (C_g), i.e. feedback loop, and follow the same procedures (1 to 7).

Result:

The current series feedback amplifier is designed and the following parameters with and without feedback are calculated.

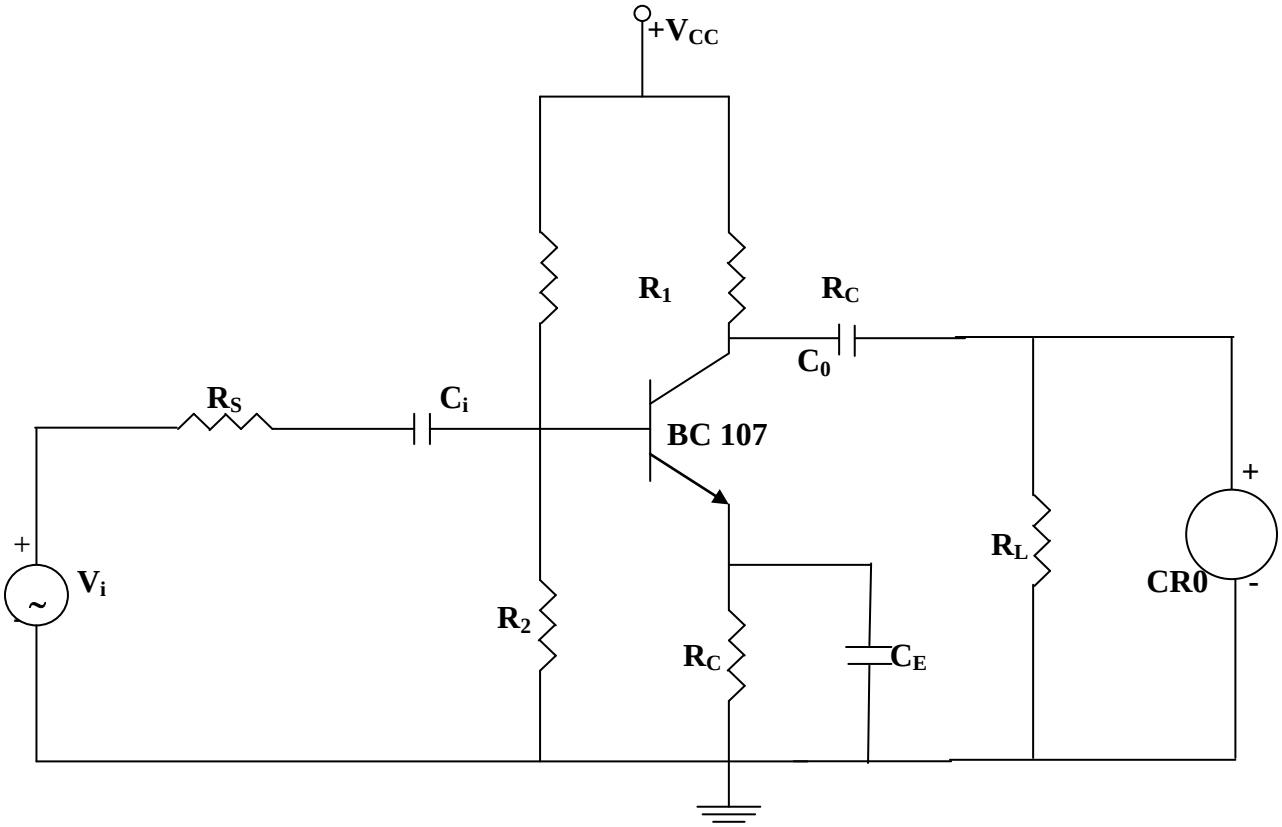
i. Mid-band gain

ii. Bandwidth and cut off frequencies

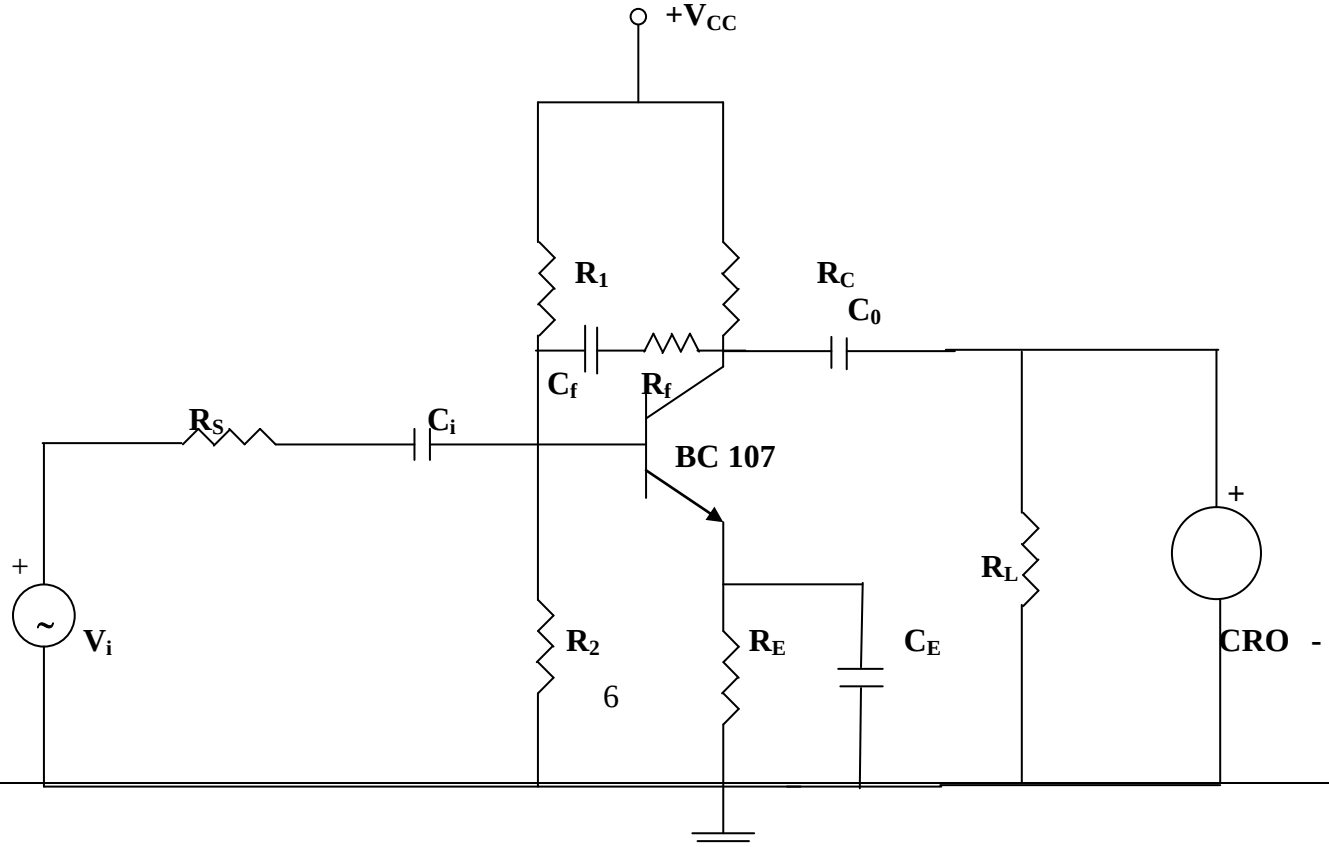
VOLTAGE-SHUNT FEEDBACK AMPLIFIER

Circuit Diagram

(i). Without Feedback



(ii). With Feedback



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Ex. No.: 1 (b) **VOLTAGE SHUNT FEEDBACK AMPLIFIERS**

Aim:

To design and test the voltage shunt feedback amplifier and to calculate the following parameter with and without feedback.

i. Mid-band gain

ii. Bandwidth and cut off frequencies

Apparatus & Components Required:

Sl. No.	Equipments & Components	Range	Quantity
1.	CRO	(0-30) MHz	1
2.	Signal Generator	(0-1) MHz	1
3.	Power Supply	(0-30) V	1
4.	Transistor	BC 107	1
5.	Capacitor	1μF, 0.5μF,	Each 2
6.	Resistor	1K, 10KΩ, 470Ω, 33KΩ, 2.2KΩ	Each 1

Theory:

To construct an amplifier with precise gain we must employ negative feedback techniques. This makes the gain to be independent of β and dependent only on the characteristics of the feedback network. It can be seen that a voltage shunt feedback amplifier results in, when the feedback resistor is connected between collector and emitter of the common emitter amplifier. The Voltage shunt feedback amplifier is employed when precise gain and low values of input and output impedances are required.

Effect of Feedback:

Output resistance - decreases, Input resistance - decreases, Gain: Trans – resistance amplifier: decreases, Bandwidth: increases, Distortion: Decreases

By making $V_o = 0$ (output opened), feedback signal becomes zero. So sampling is done for voltage. Making $V_o = 0$, the feedback signal does not become zero. In voltage shunt circuit source current (I_s) and feedback current I_f are in shunt. So the mixing is shunt. In voltage shunt input resistance R_i decreases, output resistance R_o also decreases.

Tabulation:

(i). Without Feedback

Frequency (Hz)	Output Voltage (V)	Gain = 20 log(Vo/Vin) (dB)

(ii).With Feedback

Frequency (Hz)	Output Voltage (V)	Gain = 20 log(Vo/Vin) (dB)

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set input voltage V_i = 50mV, 1KHz using signal generator.
3. Keeping the input voltage constant, vary the frequency from 0Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: Gain (dB) Vs Frequency (Hz).
5. Find the input and output impedance.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
8. Remove emitter capacitor (Ce), i.e. feedback loop, and follow the same procedures (1 to 7).

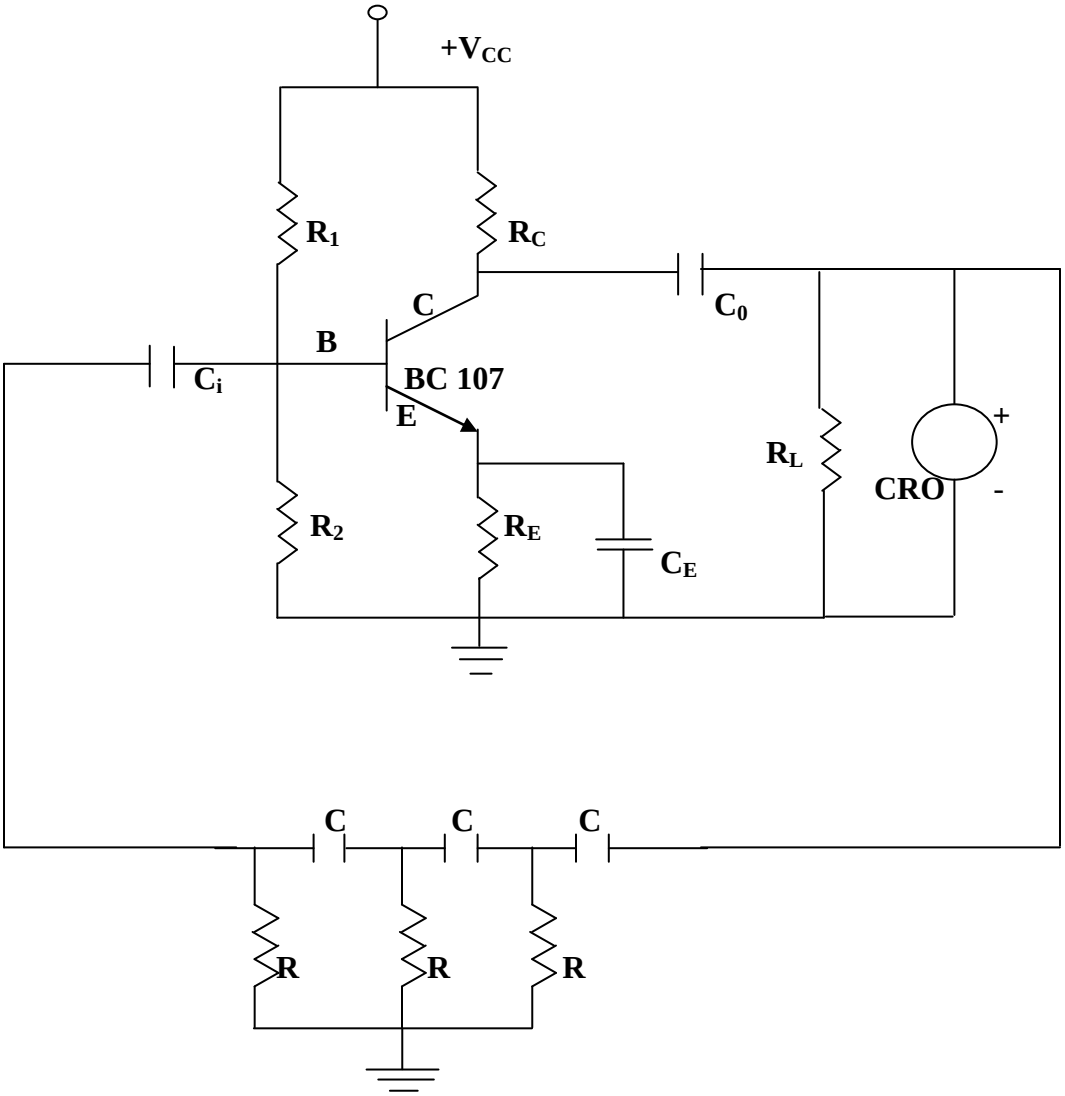
Result:

The voltage shunt feedback amplifier is designed following parameter with and without feedback.

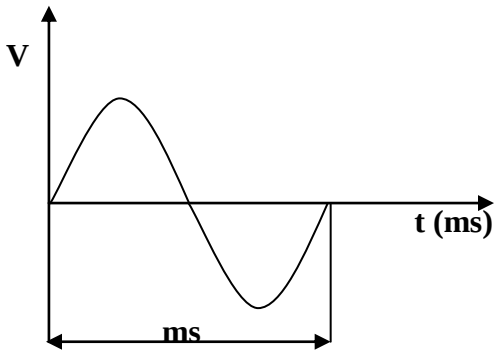
i. Mid-band gain
ii. Bandwidth and cut off frequencies are calculated

RC PHASE SHIFT OSCILLATOR

CIRCUIT DIAGRAM



MODEL GRAPH:



Ex. No.: 2 (a) **RC PHASE SHIFT OSCILLATOR**

Aim:

To design and construct a RC phase shift oscillator for given operating frequency f_o

Apparatus & Components Required:

Sl.No.	Equipments & Components	Range	Quantity
1.	CRO	(0-30) MHz	1
2.	Power Supply	(0-30) V	1
3.	Transistor	BC 107	1
4.	Capacitor	1μF, 0.5μF,0.01μF	Each 2
5.	Resistor	1K, 10KΩ, 470Ω, 33KΩ, 2.2KΩ	Each 1

RC phase shift oscillator:

$$f = 1/(2\pi RC\sqrt{6}), \quad A_V \geq -29$$

$$R_{comp} = R_i \parallel R_f$$

Theory:

RC Phase shift oscillator consists of an amplifier with three-lead network in the feedback path. Since amplifier introduces 180° phase shift between input and output, the remaining 180° phase shift is compensated by connecting three RC combination [180°/3=60° each]. If the values of R and C are so chosen that, for the given frequency f_o, the phase shift of each RC section is 60° . Thus such a RC ladder network produces a total Phase shift of 180° between its input and output voltages for the given frequency. Therefore, at the specific frequency f_o, the total phase shift from the base of the transistor around the circuit and back to the base will be exactly 360° or 0° , there by satisfying Barkhausen condition for oscillation.

$$\mathbf{f_0 = 1 / 2\pi RC\sqrt{6}}$$

The RC phase shift oscillator is suitable for audio frequencies only.

Drawbacks:

The three capacitors or resistors should be changed simultaneously to change the frequency of oscillation and it is difficult to control the amplitude of oscillation without affecting the frequency of oscillation.

Tabulation:

Parameters	Amplitude(V)	Time Period(ms)	Frequency(Hz)
Theoretical			
Practical			

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare with its theoretical frequency.

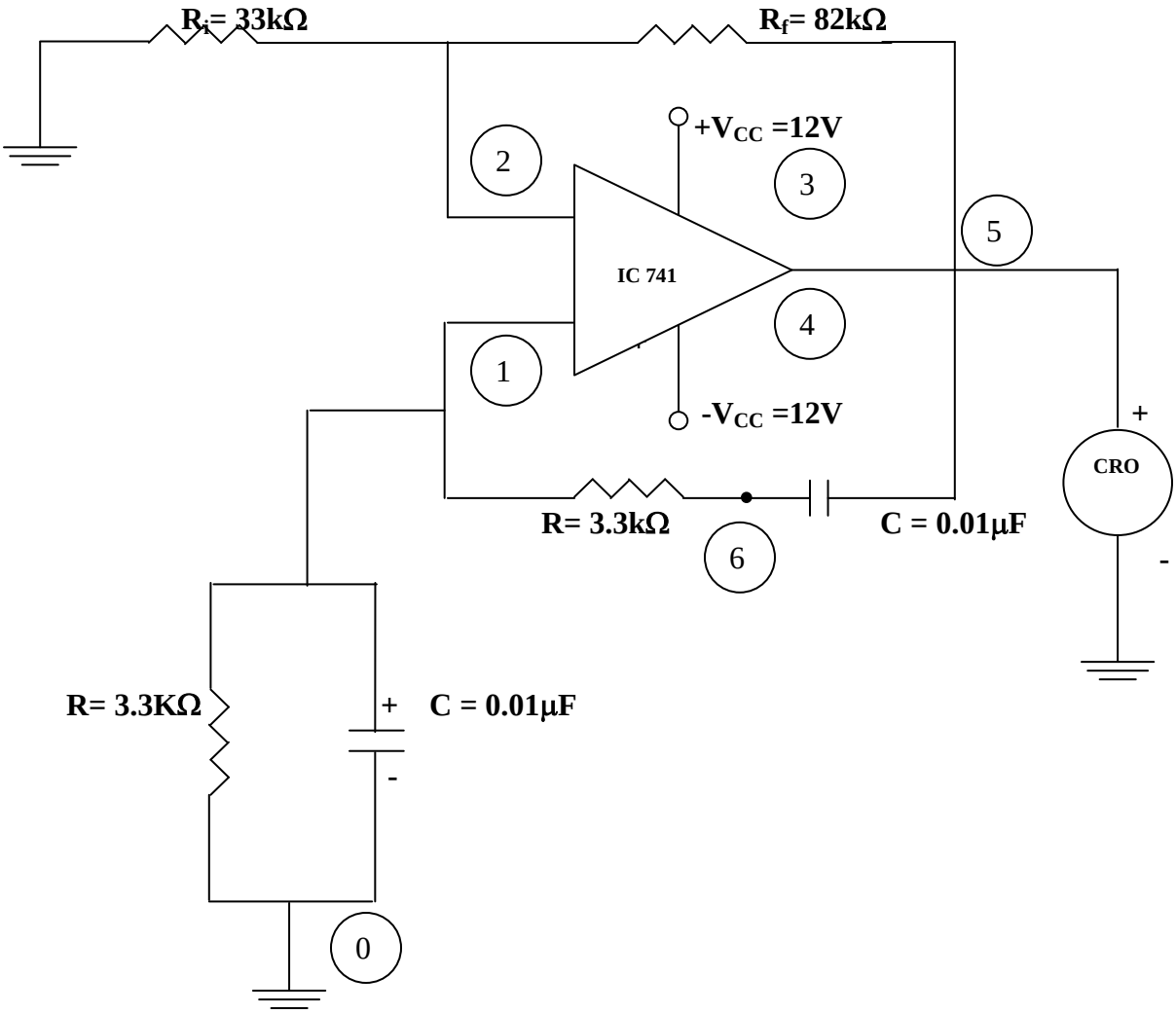
Result:

The RC phase shift oscillator for given operating frequency f_o is designed and constructed.

Parameter	Theoretical	Practical
Frequency		

WEIN BRIDGE OSCILLATOR

CIRCUIT DIAGRAM



Ex. No.: 2 (b) **WEIN BRIDGE OSCILLATOR**

Aim:

To design and test the Wein bridge oscillator-using operational amplifier

Apparatus required:

Sl. No.	Components	Specification / Range	Quantity
1.	Op-amp	IC 741	1
2.	Resistor	3.3 kΩ, 33 kΩ, 82 kΩ	2, 1, 1
3.	Capacitor	0.01μF	2
4.	CRO	(0-30) MHz	1
5.	Bread Board	-	1

Wein bridge oscillator:

$f = 1/(2\pi RC)$, $A_V \geq 3$

Theory:

Amplifier stage introduces 180°-phase shift and feedback network introduces 180° phase shift to obtain a phase shift of 360° around a loop. This is required condition for any oscillator. But Wein bridge oscillator uses a non-inverting amplifier and hence does not provide any phase shift during amplifier stage. As total phase shift is 0° in wein bridge type no phase shift is necessary through feedback. Total phase-shit around a loop is 0°

Design:-

$f = 1 / (2\pi RC)$

$f = 1 / 2 \times 3.14 \times 3.3 \times 10^{3} \times 0.01 \times 10^{-5}$

$= 4822.8Hz$

$\cong 4.8KHz$

$R_i = 10R = 33K\Omega,$

$R_f \geq 2R_1$

$R_f = 2(33K)$

$R_f \geq 82K\Omega$

Tabulation:

Derived frequency (Hz)	Observed frequency (Hz)	Amplitude(V)	Time Period(ms)

Procedure:

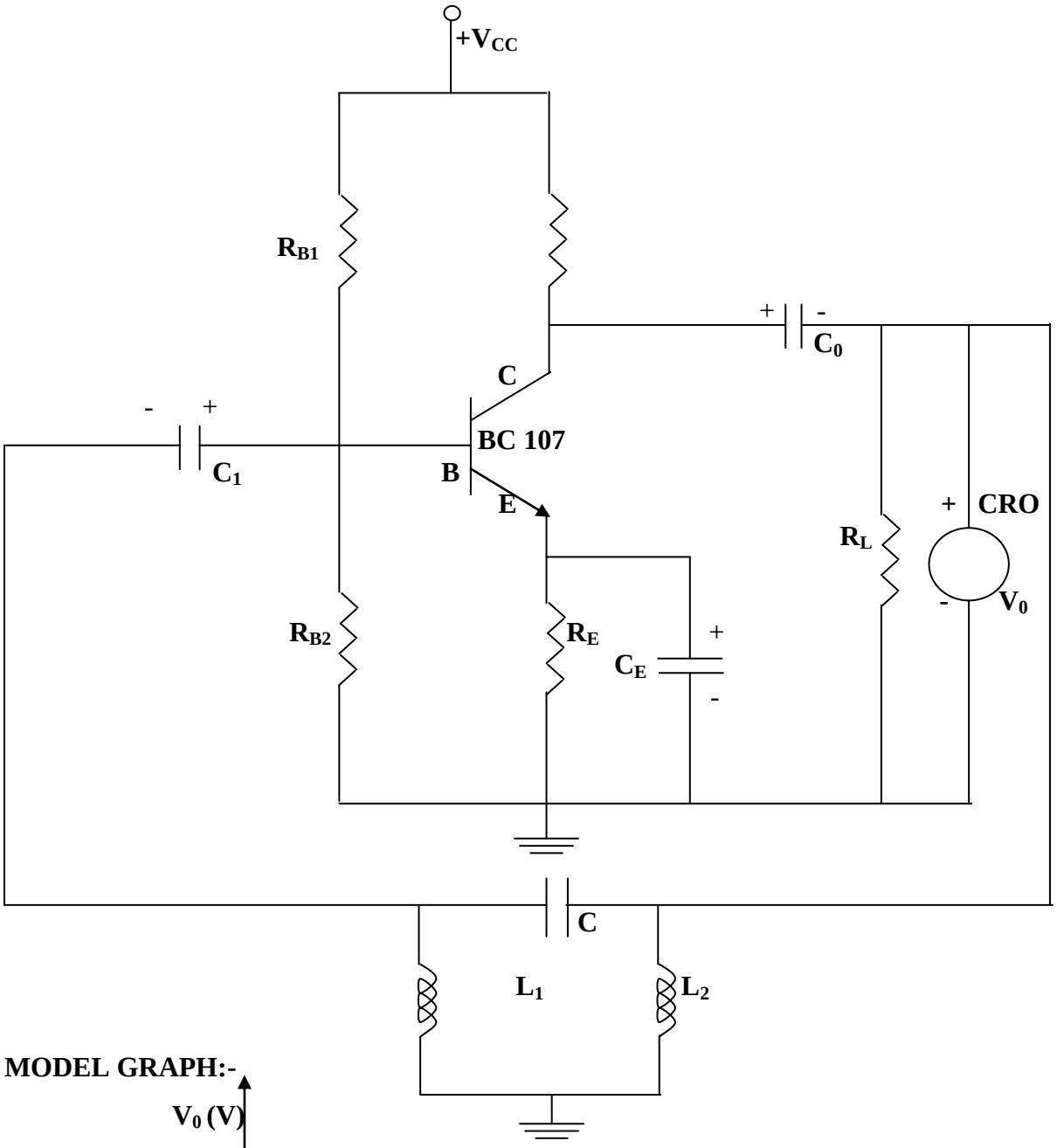
1. The circuit connections are made as per the circuit diagram
2. The time period and amplitude is noted for both oscillators.
3. Graph is plotted by taken amplitude along Y-axis and time along X-axis.

Result:

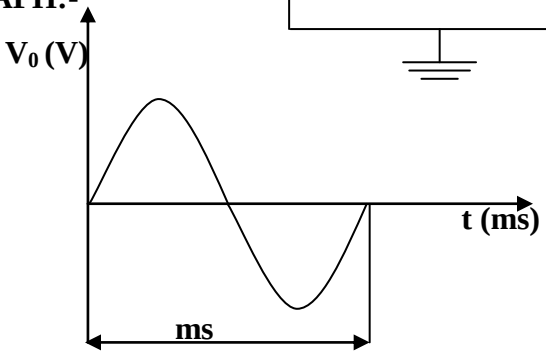
The Wein bridge oscillator using operational amplifier was designed and constructed.

HARTLEY OSCILLATOR

CIRCUIT DIAGRAM



MODEL GRAPH:-



Ex. No.: 3 (a) **HARTLEY OSCILLATOR**

Aim:

To design and construct Hartley oscillator at the giver operating frequency.

Apparatus & Components Required:

Sl. No.	Equipments & Components	Range	Quantity
1.	CRO	(0-30) MHz	1
2.	Power Supply	(0-30) V	1
3.	Transistor	BC 107	1
4.	Capacitor	1μF, 0.5μF,0.01μF, 0.1μF,1nμF	Each 2
5.	Resistor	1K, 10KΩ, 470Ω,100KΩ 33KΩ, 2.2KΩ,560Ω	Each 1
6.	Inductor	1mH, 0.4mH	Each 1

Theory:

In the CE mode, the transistor provides the phase difference of 180° between the input and output . The resistors R_1, R_2 and R_E provided the necessary dc bias to the transistor. C_E is a by pass capacitor. C_{C1} and C_{C2} are coupling capacitors. The feedback network consisting pf inductors L_1 and L_2 and capacitor C determines the frequency of oscillation. When the supply voltage $+V_{CC}$ is switched ON, a transient current is produced in the tank circuit and damped harmonic oscillations are set up in the circuit. The oscillatory current in the tank circuit produces a.c. voltages across L_1 and L_2. As terminal 3 is earthed, it is at zero potential. If terminal 1 is at a positive potential with respect to 3 at any instant, terminal 1 is at a positive potential with respect to 3 at any instant, terminal 2 will be at a negative potential with respect to 3 at the same instant. Thus the phase difference between the terminals 1 and 2 is always 180°. In the CE mode, the transistor provides the phase difference of 180° between the input and output. Therefore, the total phase shift is 360°. Thus, at the frequency determined for the tank circuit, the necessary condition for sustained oscillation is satisfied. If the feedback is adjusted so that the loop gain Aβ =1, the circuit acts as an oscillator.

The frequency of oscillation is $f_o = 1 / 2\pi\sqrt{LC}$, where $L = L_1 + L_2 + 2M$, and M is the value of mutual inductance between coils L_1 and L_2. The condition for sustained oscillation is

$$\mathbf{h_{fe} \geq (L_1 + M) / (L_2 + M)}$$

Tabulation:

Amplitude(V)	Time Period(ms)	Frequency(Hz)	
		Theoretical	Observed

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare with its theoretical frequency.

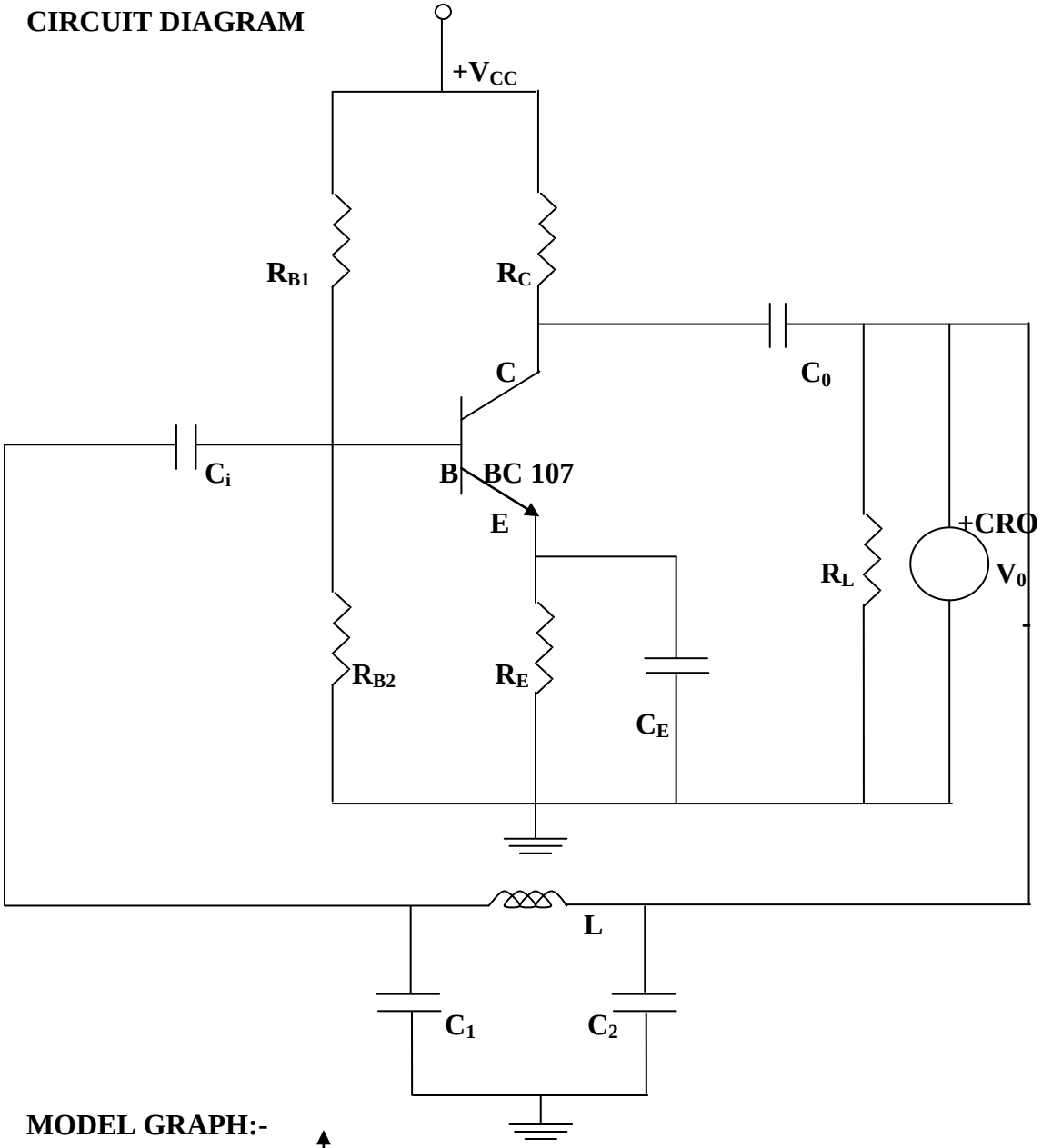
Result:

The Hartley oscillator for the given operating frequency is designed and constructed.

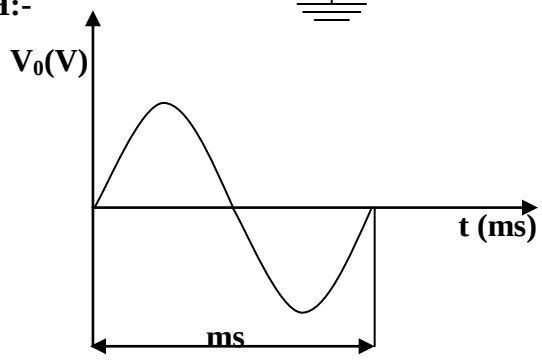
Parameter	**Theoretical**	**Practical**
Frequency		

COLPITTS OSCILLATOR

CIRCUIT DIAGRAM



MODEL GRAPH:-



Ex. No.: 3 (b) **COLPITTS OSCILLATOR**

Aim:

To design and construct Colpitts oscillator at the given operating frequency.

Apparatus & Components Required:

Sl.No.	Equipments & Components	Range	Quantity
1.	CRO	(0-30) MHz	1
2.	Power Supply	(0-30) V	1
3.	Transistor	BC 107	1
4.	Capacitor	1μF, 0.5μF,0.01μF, 0.1μF,1nμF	Each 2
5.	Resistor	1K, 10KΩ, 470Ω,100KΩ 33KΩ, 2.2KΩ,560Ω	Each 1
6.	Inductor	1mH, 0.4mH, 5mH	Each 1

Theory:

The resistors R_1, R_2 and R_E provided the necessary dc bias to the transistor. C_E is a by pass capacitor. C_{C1} and C_{C2} are coupling capacitors. The feedback network consisting of capacitors C_1 and C_2 and an inductor L determines the frequency of oscillation. When the supply voltage $+V_{CC}$ is switched ON, a transient current is produced in the tank circuit and damped harmonic oscillations are set up in the circuit. The oscillatory current in the tank circuit produces a.c. voltages across C_1 and C_2. As terminal 3 is earthed, it is at zero potential. If terminal 1 is at a positive potential with respect to 3 at any instant, terminal 1 is at a positive potential with respect to 3 at any instant, terminal 2 will be at a negative potential with respect to 3 at the same instant. Thus the phase difference between the terminals 1 and 2 is always 180°. In the CE mode, the transistor provides the phase difference of 180° between the input and output. Therefore, the total phase shift is 360°. Thus, at the frequency determined for the tank circuit, the necessary condition for sustained oscillation is satisfied. If the feedback is adjusted so that the loop gain Aβ =1, the circuit acts as an oscillator.

The frequency of oscillation is $f_o = 1 / 2\pi\sqrt{LC}$, where $1/C = 1/C_1 + 1/C_2$, . The condition for sustained oscillation is

$$\mathbf{h_{fe} = C_2 / C_1}$$

It is widely used in commercial signal generators for frequencies between 1MHz and 500MHz.It is also used as a local oscillator in super heterodyne radio receiver.

Tabulation:

Amplitude (V)	Time (ms)	Theoretical frequency (H_2)	Practical frequency (H_z)

Tabulation:

Input	Amplitude(V)	Time Period(ms)
VC_1		
VC_2		

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare with its theoretical frequency.

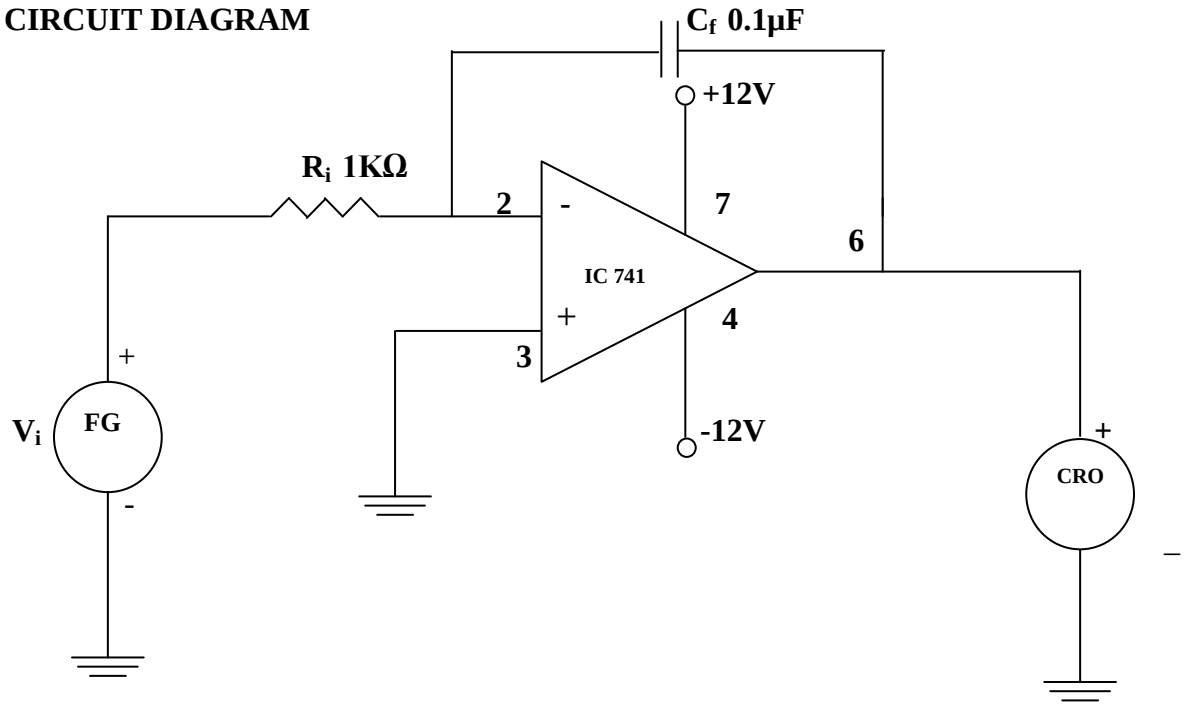
Result:

The Colpitts oscillator at the given operating frequency is designed and constructed.

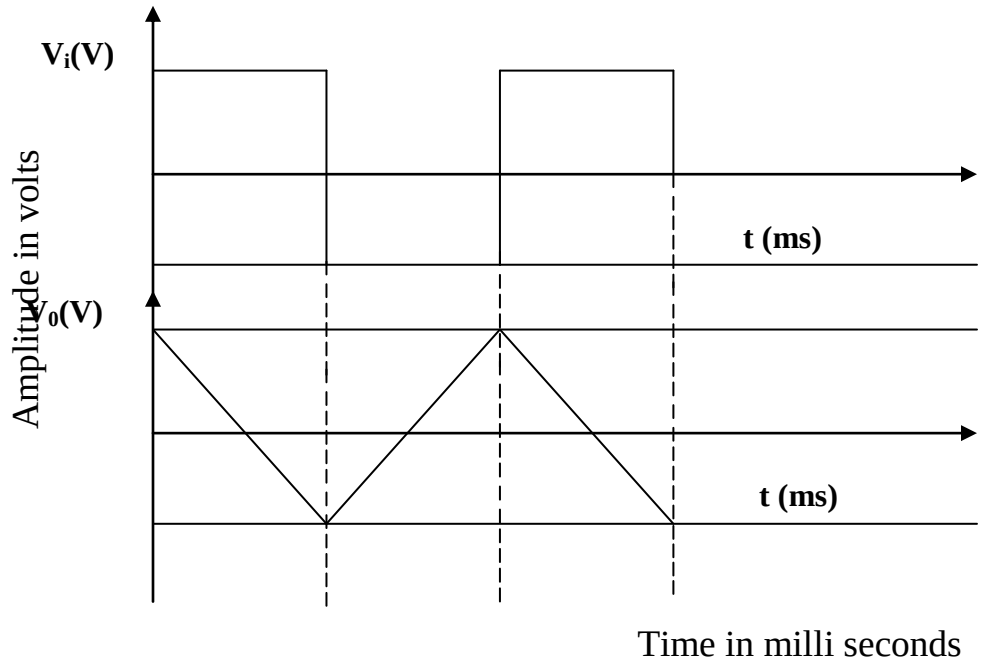
Parameter	**Theoretical**	**Practical**
Frequency		

(A) INTEGRATOR

CIRCUIT DIAGRAM



Model Graph:-



Tabulation:

Waveform	**Amplitude (V)**	**Time Period (ms)**
Input (V_i) Output (V_0)		

Ex. No.: 4 **RC INTEGRATOR AND DIFFERENTIATOR USING OP AMP**

Aim:

To construct and test the RC Integrator and Differentiator circuit using operational amplifier**.**

Apparatus required:

S.NO	Components	Range	Quantity
1.	Op-amp	IC741	1
2.	Resistors, capacitors	1k,1µF	Each 1
3.	CRO	(0-30)MHz	1
4.	Dual power supply	±12V,2A	1
5.	Bread board	-	1
6.	Function generator	(0-1)MHz	1
7.	Connecting Wires	-	Required

Theory:

Differentiator:

The circuit that performs the mathematical operations of differentiation i.e. the output waveform is the derivative of the input waveform.

Output voltage $\mathbf{V_O = - R_f . C_1 (dV_i / dt)}$

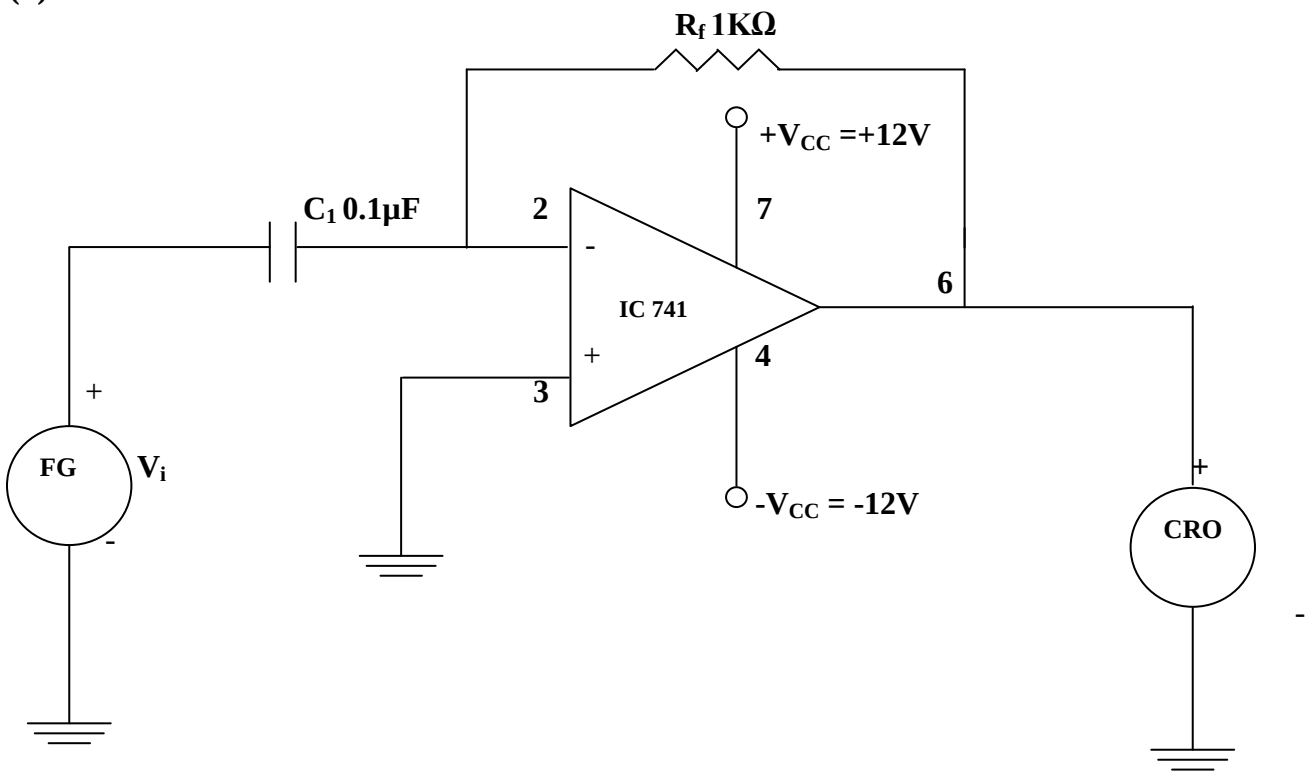
Thus the output voltage V_O is a constant ($-R_f C_1$) times the derivate of the input voltage V_i and the circuit is a differentiator. The minus sign indicates a 180 phase shift of the output waveform V_O with respect to the input signal.

Integrator:

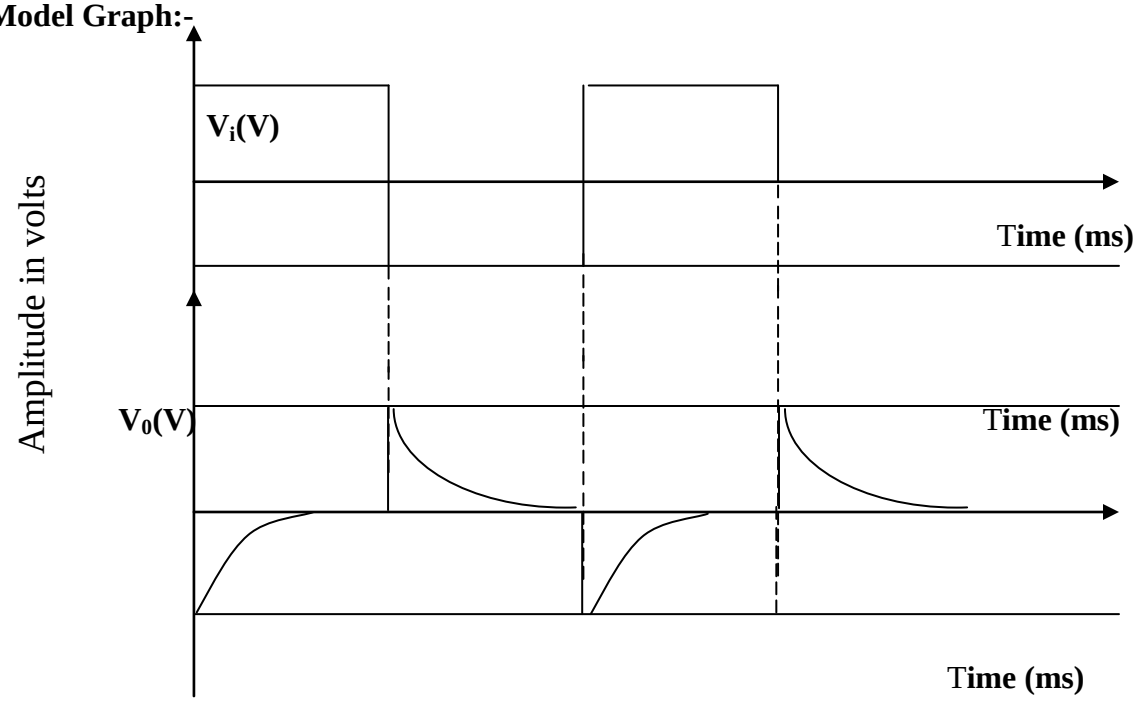
A simple low pass RC circuit can also work as an integrator when time constant is very large. This requires very large values of R and C. The components R and C cannot be made infinitely large because of practical limitations. However in the op-amp integrator by Miller's theorem, the effective input capacitance becomes $C_f (1-A_V)$ where A_v is the gain of-amp.The gain A_V is the gain of the op-amp. The gain A_V is infinite for an ideal op-amp.So the effective time constant of the op-amp integrator becomes very large which results in perfect integration.

$$\text{Output voltage, } V_O = [-1 / (R_i C_f)] \int_0^{\alpha} V_i \, . \, dt$$

(b) Differentiator:-



Model Graph:-



Tabulation:

Waveform	Amplitude (V)	Time Period (ms)
Input (V_i) Output (V_0)		

Procedure:

1. Circuit connections are given as per the circuit diagram.
2. For both inverting and non-inverting amplifier the input voltage, output voltage and time period is noted.
3. Input and output waveforms are drawn in a graph.

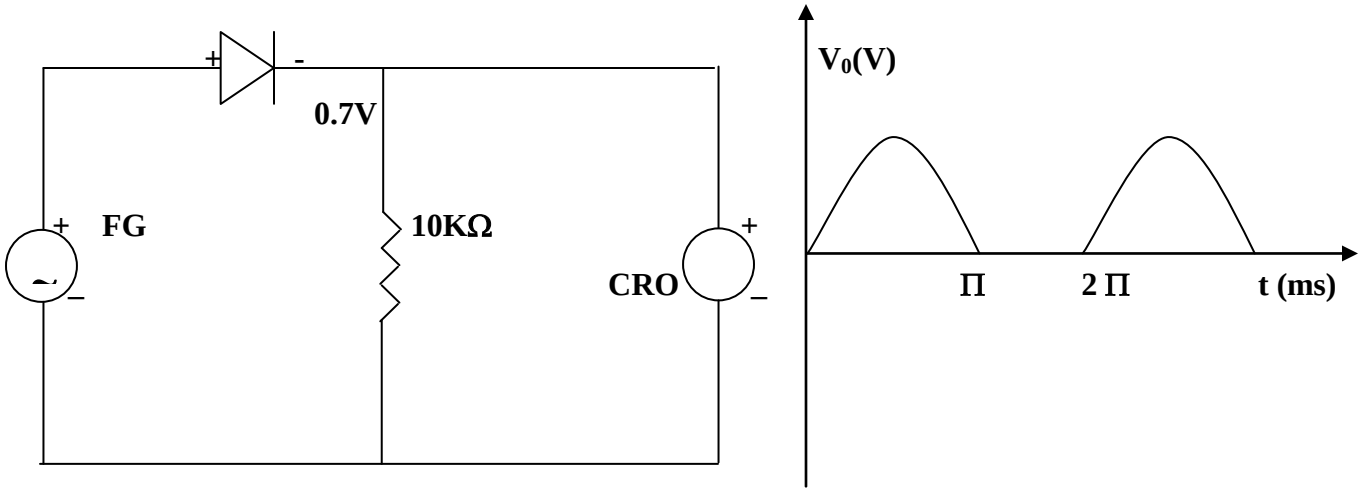
Result:

Thus the integrator and differentiator is designed using operational amplifier**.**

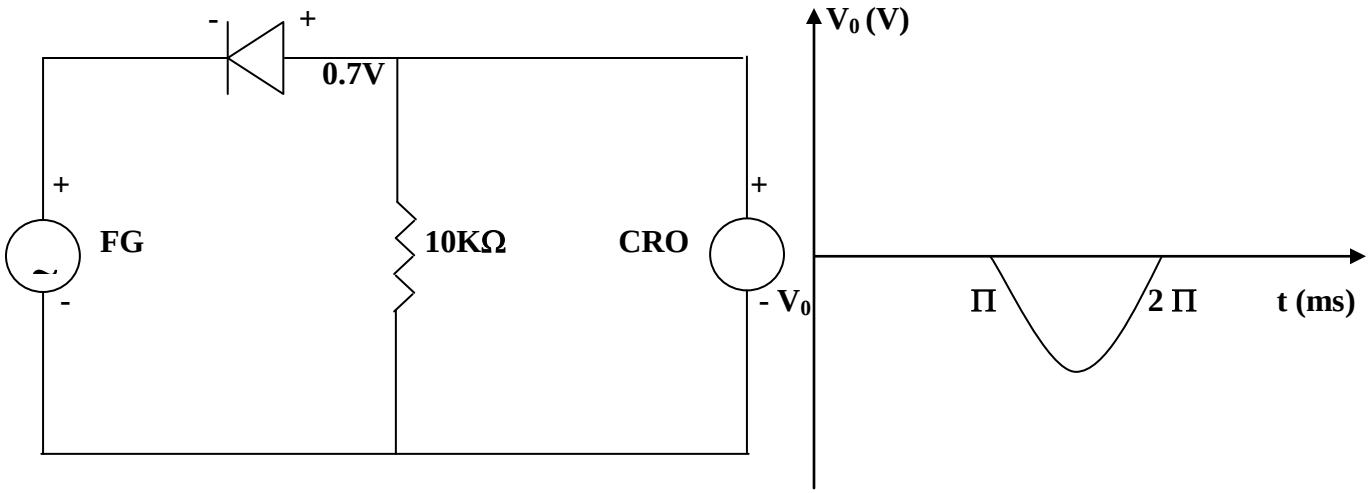
CLIPPER

CIRCUIT DIAGRAM

Negative Clipper



Positive Clipper



Ex. No.: 5(a) **CLIPPERS**

Aim:

To observe the clipping waveforms with different clipping configurations.

Apparatus & Components Required:

Sl. No.	Equipments & Components	Range	Quantity
1.	CRO	(0-30) MHz	1
2.	Signal Generator	(0-3) MHz	1
3.	Power Supply	(0-30) V	1
4.	Diode	IN 4007	1
5.	Resistor	10KΩ	1

Theory:

The circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform are called clipper circuits or clippers, Clipping or limiting circuits are designed to reduce the positive and /or negative extremities of an input waveform to a pre determined value which may be zero.

Tabulation:

Parameters	Input	Output	
		Positive Clipper $RC << \tau$	**Negative Clipper** $RC << \tau$
Amplitude(V)			
Time Period(ms)			

Procedure:

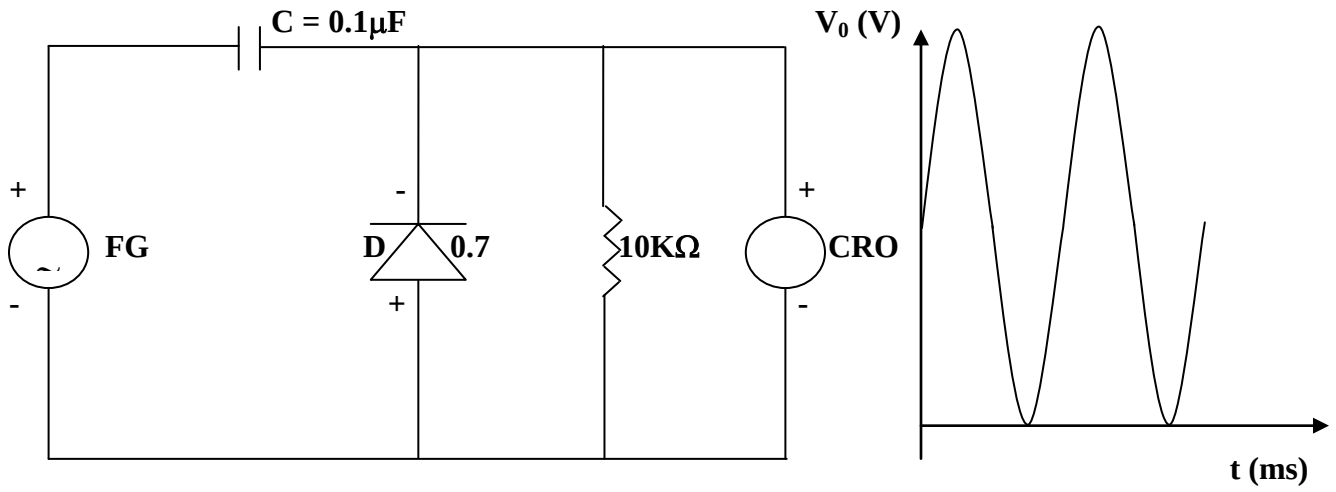
1. Connect the circuit as per the circuit diagram.
2. Set input voltage V_i = 5V, 1Khz using signal generator.
3. Observe the output wave form using CRO. (DC – mode)
4. Sketch the observed waveform on the graph sheet.

Result:

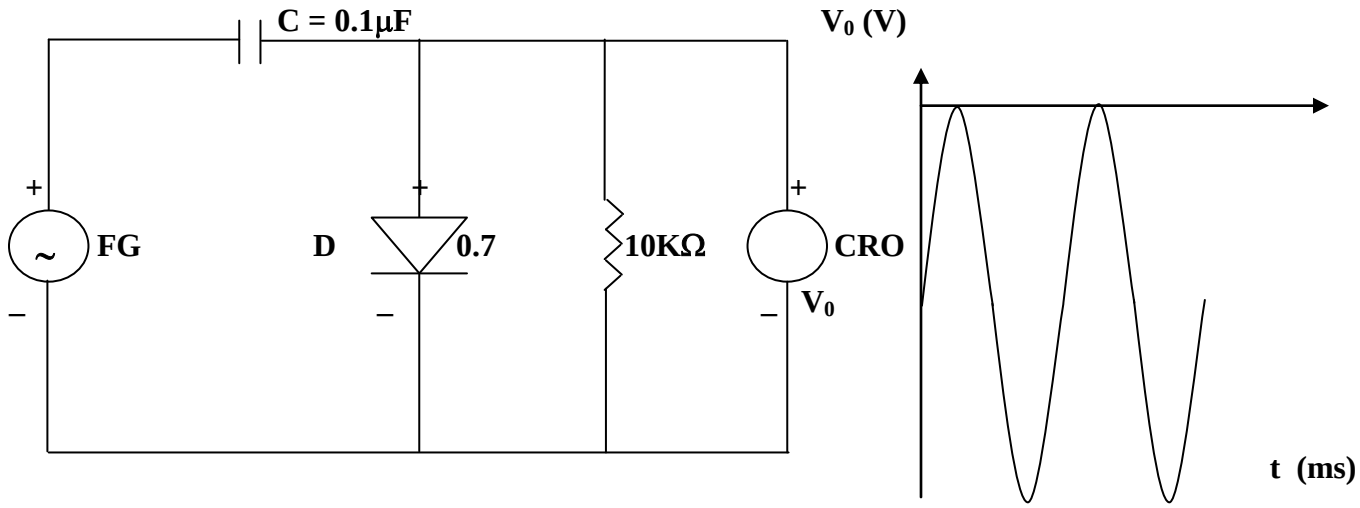
The clipping waveforms in different clipping configurations are observed.

CLAMPERS

POSITIVE CLAMPERS:-



NEGATIVE CLAMPERS:-



Ex. No.: 5(b) **CLAMPER CIRCUITS**

Aim:

To observe the clamping waveform in different configuration.

i. Positive clamping circuits

ii. Negative clamping circuits

Apparatus &Components Required:

Sl. No.	Equipments & Components	Range	Quantity
1.	CRO	(0-30) MHz	1
2.	Signal Generator	(0-1) MHz	1
3.	Power Supply	(0-30) V	1
4.	Diode	IN 4007	1
5.	Capacitor	0.1μF	1
6.	Resistor	10KΩ	1

Theory:

Introducing a dc level into an ac signal or shifting the ac signal to a predetermined dc level other than zero is called dc clampers/restorers.

Tabulation:

Parameters	Input	Output	
		Positive Clipper $RC << \tau$	**Negative Clipper** $RC << \tau$
Amplitude (V)			
Time Period (ms)			

Procedure:

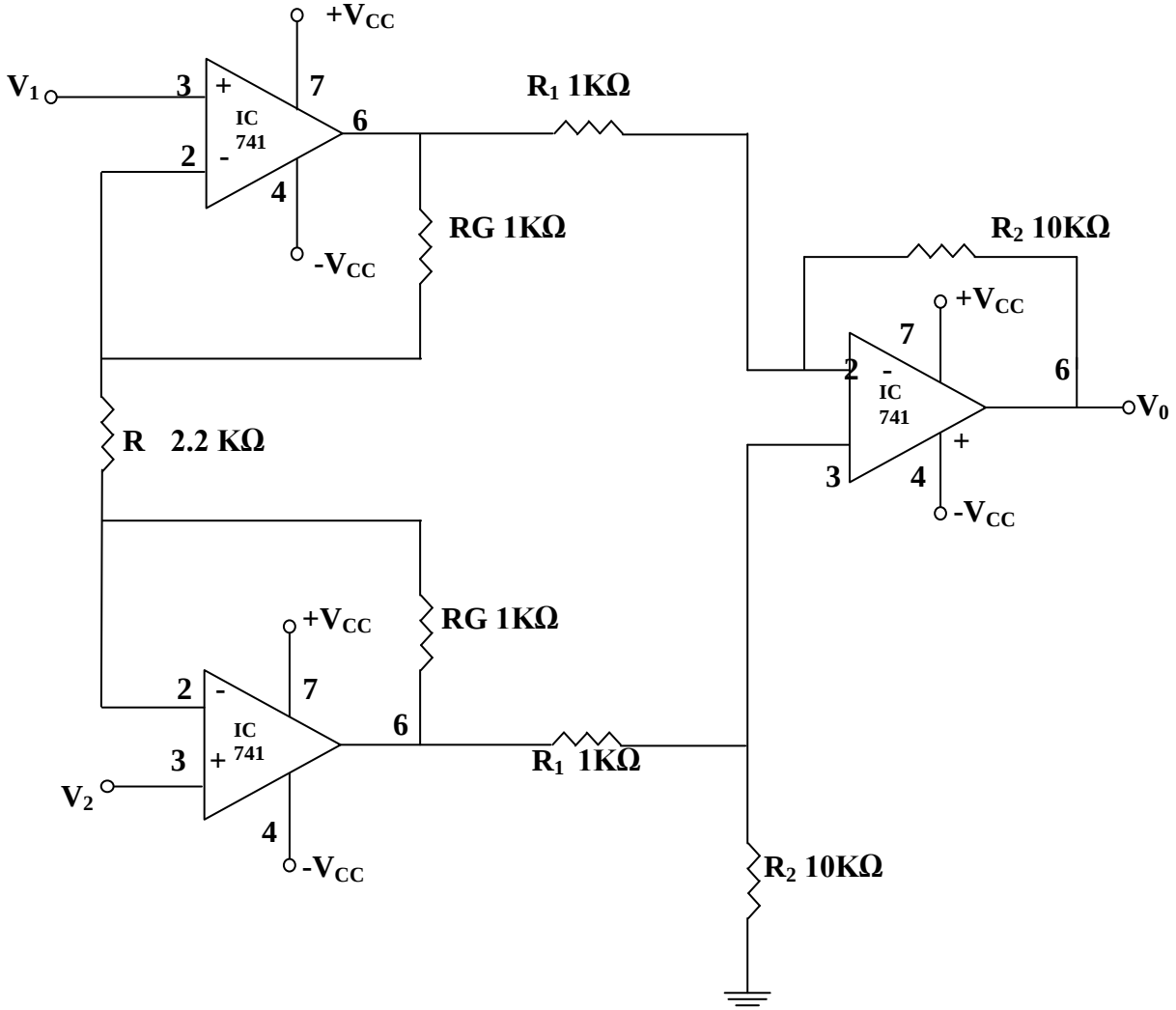
1. Connect the circuit as per the circuit diagram.
2. Set input voltage V_i = 5V, 1Khz using signal generator.
3. Observe the output wave form using CRO. (DC – mode)
4. Sketch the observed waveform on the graph sheet.

Result:

The clamping waveform in different configurations is observed.

INSTRUMENTATION AMPLIFIER

Circuit Diagram:-



Ex. No.: 6 **INSTRUMENTATION AMPLIFIERS**

Aim:

To design and construct, the instrumentation amplifier, using operational amplifier.

Apparatus required:

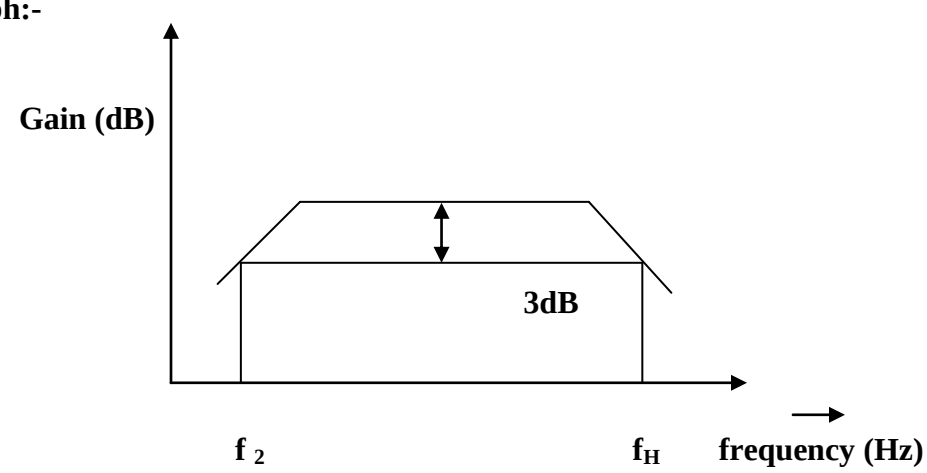
S.NO	Components	Range	Quantity
1.	Resistors	1kΩ,10kΩ	Each 2
2.	Op-amp	IC 741	3
3.	CRO	(0-30)MHz	1
4.	Function generator	(0-1)MHz	2
5.	Bread board	-	Required

Theory:

- The measurement of the physical quantities is generally carried out with the help of a device called as transducer.
- A transducer is a device, which converts one form of energy into another.
- The special amplifier which is used for low level amplification with high CMRR high input impedance to avoid loading low power consumption and is called an instrumentation amplifier.
- Such special featured instrumentation amplifiers have become an integral part of modern testing and measurement instrumentation.
- Requirements of a good instrumentation amplifier is finite, accurate and stable gain, easier gain adjustment, high input impedance low output impedance, high CMRR, Low power consumption, Low thermal and time drift, high slew rate.

$$\text{Voltage } V_o = \frac{R_2}{R_1}\left(1 + \frac{2R_G}{R}\right)(V_2 - V_1)$$

Model Graph:-



Tabulation

$V_i = (V_2 - V_1)$

Frequency (Hz)	O/P Voltage V_0(V)	Gain (dB) = 20 log (V_0 /V_i)

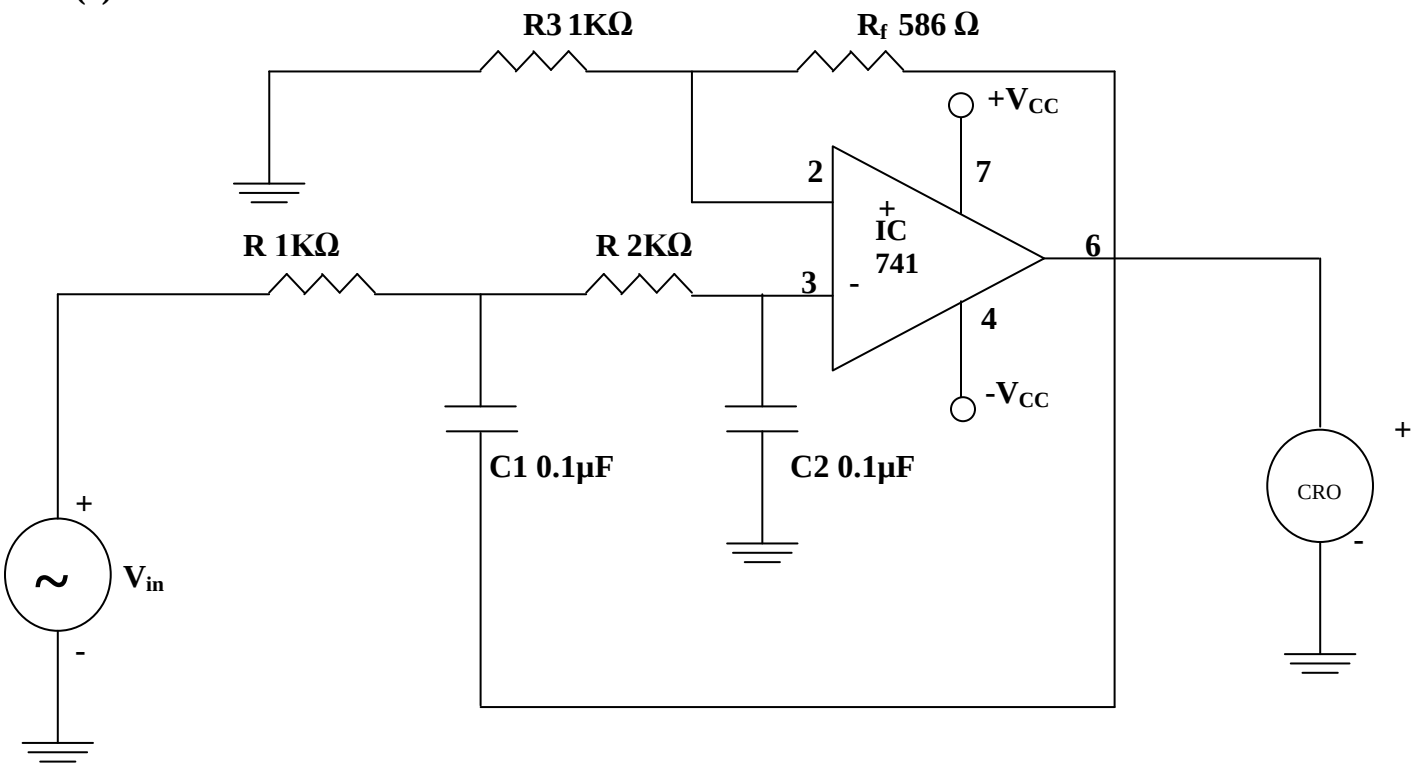
Procedure:

- Connections are made as per the circuit diagram.
- Inputs are applied at Non-inverting terminals of input op-amp
- Output of amplifier (Amplitude and time) is noted.
- The theoretical and practical frequency was calculated.
- The graph is plotted against gain and amplitude.

Result:

Thus the instrumentation amplifier is constructed and output waveform is observed**.**

(a) Low Pass Filter:-



Model Graph:-

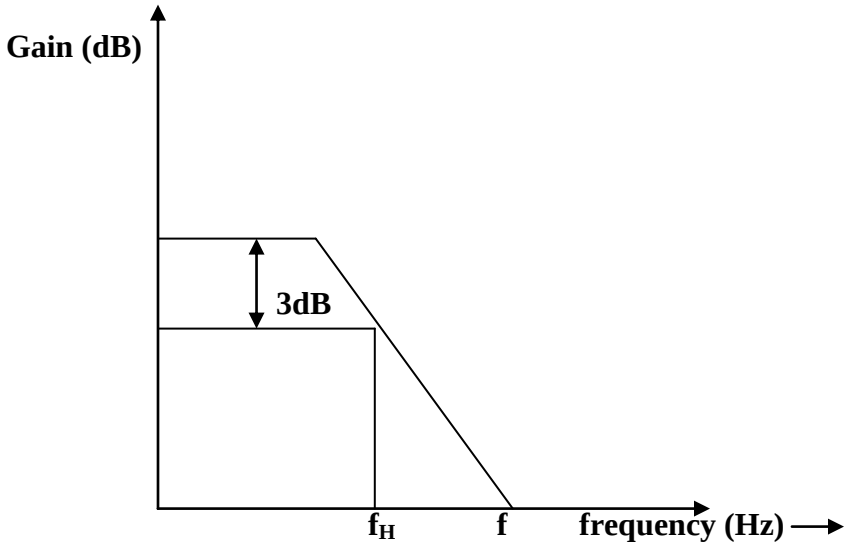


Table:-

V_{in} =

Frequency (Hz)	O/P Voltage V_0(V)	Gain (dB) = 20 log (V_0 /V_i)

Ex. No.: 7 ACTIVE LOW PASS FILTER, HIGH PASS FILTER AND BAND PASS FILTER

Aim:

To construct and test the Active low pass filter, High pass filter and Band pass filter using operational amplifier.

Apparatus required:

S.NO	Components	Range	Quantity
1.	IC	IC 741	2
2.	Resistors	10KΩ, 20kΩ	1
3.	Capacitor	1μF	1
4.	CRO	(0-30) MHz	1
5.	Function generator	(0-300) MHz	1
6.	Bread board		
7.	Connecting wires		Required

Design:

Low pass filter:

Gain $A_0 = 1 + R_f / R_2$

Frequency $f_0 = 1/2\pi RC$

Gain $A_0 = 3 - \alpha$

$\alpha = 1.414$

High pass filter:

Gain $A_0 = 1 + R_f / R_3$

Frequency $f_0 = 1 / 2\pi RC$

Gain $A_0 = 3 - \alpha$

Band pass filter:

Resistor $R_1 = 1/2\pi f_L C$, f_L-Lower cut off frequency

Resistor $R_2 = 1/2\pi f_H C$, f_H-Upper cut off frequency

Gain $A_0 = A_{01} \times A_{02}$

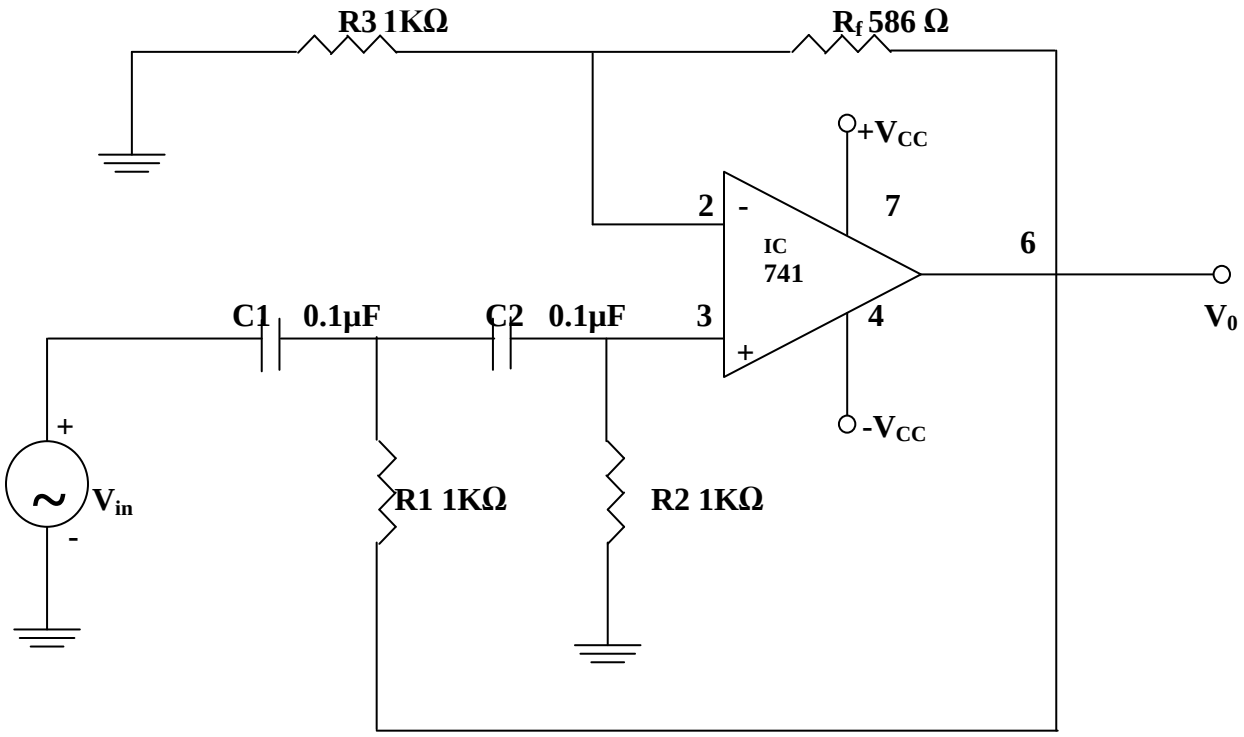
Gain $A_{01} = 1 + R_f / R_2$

Gain $A_{02} = 1 + R_f / R_3$

Bandwidth $B.W = f_H - f_L$

Quality factor $Q = f_C / BW$

(b) Active High Pass Filter:-



Model Graph:-

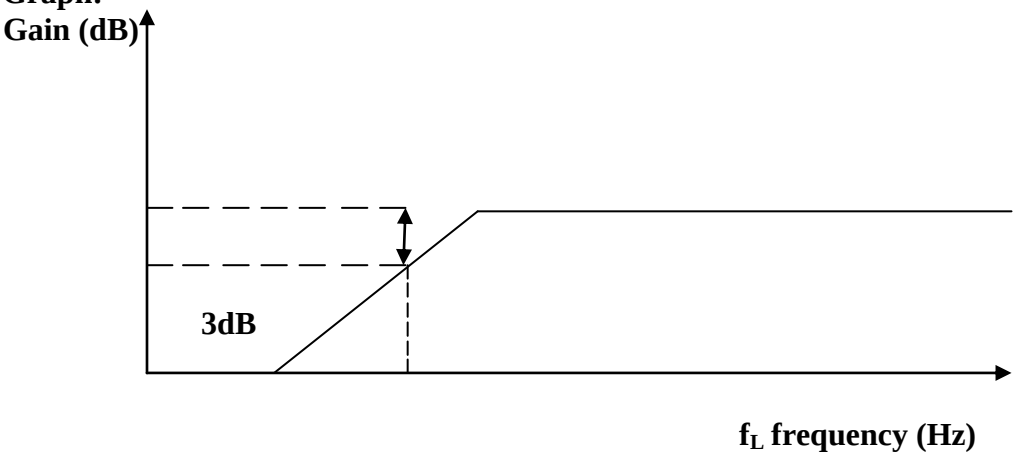


Table:- V_i =

Frequency (Hz)	O/P Voltage V_0(V)	Gain (dB) = 20 log (V_0 /V_i)

Theory:

Low pass filter:

- A filter is a circuit that is designed to pass a specified band of frequencies while attenuating all the signals outside that band.
- It is a frequency selective circuit.The practical response of the filter must be very close to an ideal one.
- In case of low pass filter, it is always desirable that the gain rolls of very fast after the cut off frequency in the stop band.

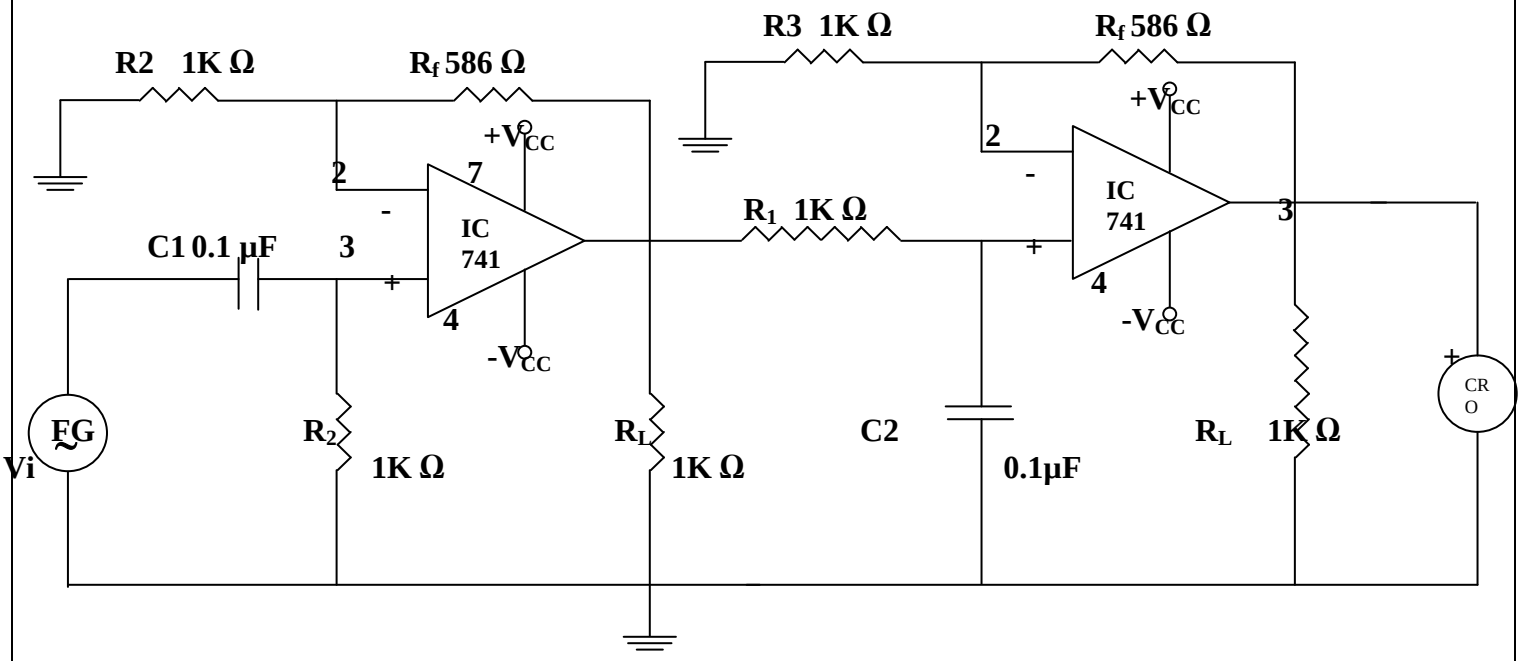
High pass filter:

- A filter is a circuit that is designed to pass a specified band of frequencies while attenuating all the signals outside that band.

Band pass filter:

- A band pass filter is basically a frequency selector. The pass band, which is between f_H and f_L is called bandwidth of the filter.
- The frequency at the center of the pass band is called center frequency (f_C).
- The gain is maximum at f_C and it is denoted as total pass band gain.

(c) Band Pass Filter:-



Model Graph:-

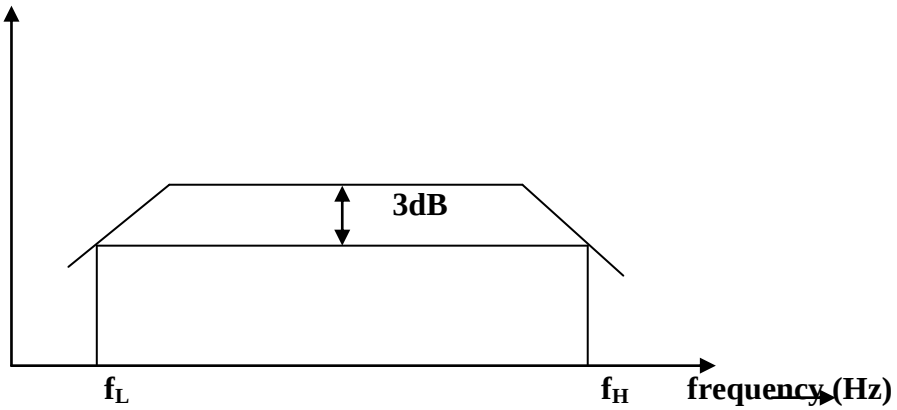


Table:-

V_i =

Frequency (Hz)	O/P Voltage V_0(V)	Gain (dB) = 20 log (V_0 /V_i)

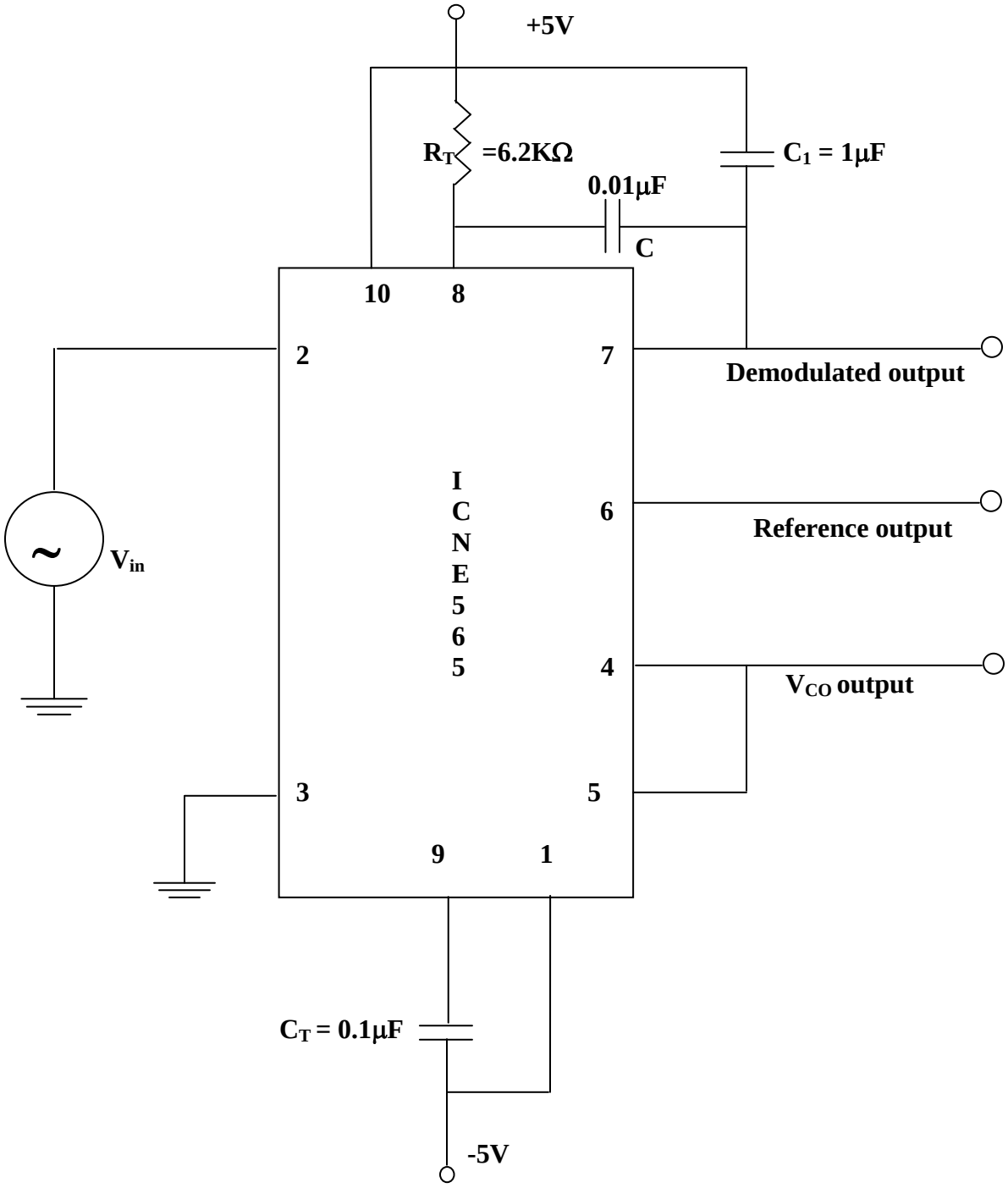
Procedure:

- Connections are made as per the circuit diagram.
- Input voltage is set and the output waveform is obtained in the CRO.
- By varying the frequency, the amplitude of output wave is noted.
- The readings are taken for different frequency.
- Graph is plotted between gain in dB on Y –axis and frequency in X -axis.

Result:

Thus the low pass, high pass and band pass filter was designed and frequency response curve is observed.

CIRCUIT DIAGRAM:-



Ex. No.: 8 PLL CHARACTERISTICS AND ITS USE AS FREQUENCY MULTPLIER, CLOCK SYNCHRONIZATION

Aim:

To construct and test the PLL characteristics and its use as frequency multplier, clock synchronization.

Apparatus required:

S.NO	Components	Range	Quantity
1.	IC	NE 565	1
2.	Resistor	6.8KΩ	1
3.	Capacitor	0.1 µF,0.01 µF,1 µF	Each 1

Theory:

- IC 565 PLL consists of phase detector amplifier and low pass filter and V_{CO}. The phase locked feedback loop is not internally connected.
- Therefore it is necessary to connect output of V_{CO} (pin4) to the phase comparator input (pin5) externally.
- In frequency multiplication applications a digital frequency divider is inserted into the loop i.e. between pin 4 and pin 5.
- The center frequency of the PLL is determined by the free running frequency of the V_{CO} and it is given as.

$$\textbf{Frequency } f_0 = 0.25 / R_T C_T, \Delta f_L = 7.8 f_0 / 10$$

- Where Resistor R_1 and capacitor C_1 are an external resistor and a capacitor connected to pin 8 and 9 respectively.
- The values of R_1 and C_1 are adjusted such that the free running frequency will be at the center of the input frequency range.
- The value of R_1 is restricted from 2KΩ but a capacitor can have any value. A capacitor can have any value. A capacitor C_2 connected between pin 7 and the positive supply (pin10).

- The lock range $\mathbf{f_L = \pm 8 f_0 / VHz}$

  $\mathbf{f_0 =}$ **Free running frequency**

  $\mathbf{\Delta f_C = \pm \sqrt{\Delta f_L / 2\pi C_T \times 3.6 \times 10^3}}$

- Lock range increases with an increase in input voltage but decreases with increases in supply voltage.
- The two inputs (pin 2 and pin 3) to the phase detector allow direct coupling of an input signals provided that there is no DC voltage difference between the pins and the DC resistance see from pin 2 pine 3 are equal.
- A reference voltage at pin 6 is approximately equal to the DC voltage of the demodulated output at pin 7.

Procedure:

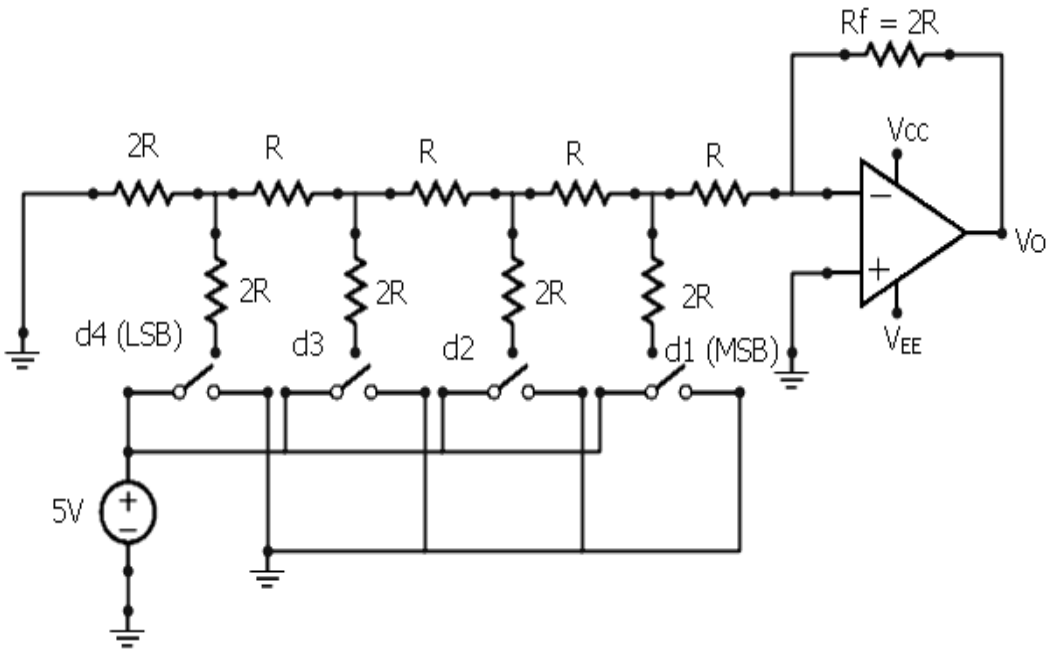
- Connections are made as per the circuit diagram.
- Measure the free running frequency of V_{CO} pin 6 with I/P signal. V_{in} set equal to zero compare it with the calculated value = $\mathbf{0.25/R_TC_T}$
- Now apply the input signal of VPP square wave at a 1K to pin 2 connect are changed of the slope to pin 3 and display this signal on the slope.
- Gradually increase the input frequency till the PLL is locked to the input frequency. It gives the lower and of the capture ranges go to increased signal input frequency till PLL gives the upper end of the lock range. It input frequency is increased further the loop will get unlocked.
- Now gradually increases the input frequency till the PLL is gain locked.
- The lock range $\mathbf{\Delta f_L = [f_2\text{-}f_4]}$ compare it with the calculated value of $\mathbf{\pm 7.8/12=f_0}$. Also the capture range is $\mathbf{\Delta f_C = f3\text{-}f_1}$ compare it the calculated value of capture range.

$$\textbf{Capture frequency } \Delta f_C = \pm \sqrt{[\Delta f_1 / 2\pi x 3.6 x 10^3 x C]}$$

Result:

Thus the PLL characteristic was constructed and the lock range and capture range was noted.

CIRCUIT DIAGRAM:-



Calculations:

Output Voltage is given by

$$\mathbf{Vo = - V_R * (Rf / 2R) * (d1/2 + d2/4 + d3/8 + d4/16)}$$

where, $V_R = 5V$,

Rf = 2R , d1 (MSB bit) and d4 (LSB bit)

Let R = 12KΩ , then

Resolution = V_{FS} / (2^n - 1) ,

Where, n= no of digital inputs

V_{FS} = Value of analog output when digital input is 1111.

Resolution = 0.3125 = Value of LSB bit.

Ex. No.: 9 R-2R LADDER TYPE D- A CONVERTER USING OP-AMP.

Aim:

Design of R/2R ladder 4-bit D/A Converter using IC 741.

Apparatus required:

S.NO	Components	Range	Quantity
1.	Op-amp	IC 741	1
2.	Capacitor	1μF	2
3.	Resistors	10KΩ, 20kΩ	8
4.	Diode	BY 127	2
5.	CRO	(0-30) MHz	1
6.	Dual power supply	± 12v	1

Theory:

- The R-2R ladder network is commonly used for Digital to Analogue conversions.
- In basic N bit R-2R resistor ladder network the digital inputs or bits range from the most significant bit (MSB) to the least significant bit (LSB).
- The bits are switched between either 0V or V_R and depending on the state and location of the bits Vo will vary between 0V and V_R .
- The MSB causes the greatest change in output voltage and the LSB causes the smallest.
- The R-2R ladder is inexpensive and relatively easy to manufacture since only two resistor values are required.
- It is fast and has fixed output impedance R. In R-2R ladder type D to A converter, only two values of resistor is used (i.e. R and 2R).
- Hence it is suitable for integrated circuit fabrication. The typical values of R are from 2.5K to 10K . In this output voltage is a weighted sum of digital inputs.
- Since the resistive ladder is a linear network, the principle of super position can be used to find the total analog output voltage for a particular digital input by adding the output voltages caused by the individual digital inputs.
- The output voltage is linearly proportional to the digital input and the range can be adjusted by changing the reference voltage V_R .

Observation table :

d1	d2	d3	d4	Vo (observed)	Vo (Calculated)
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
1	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

Procedure:

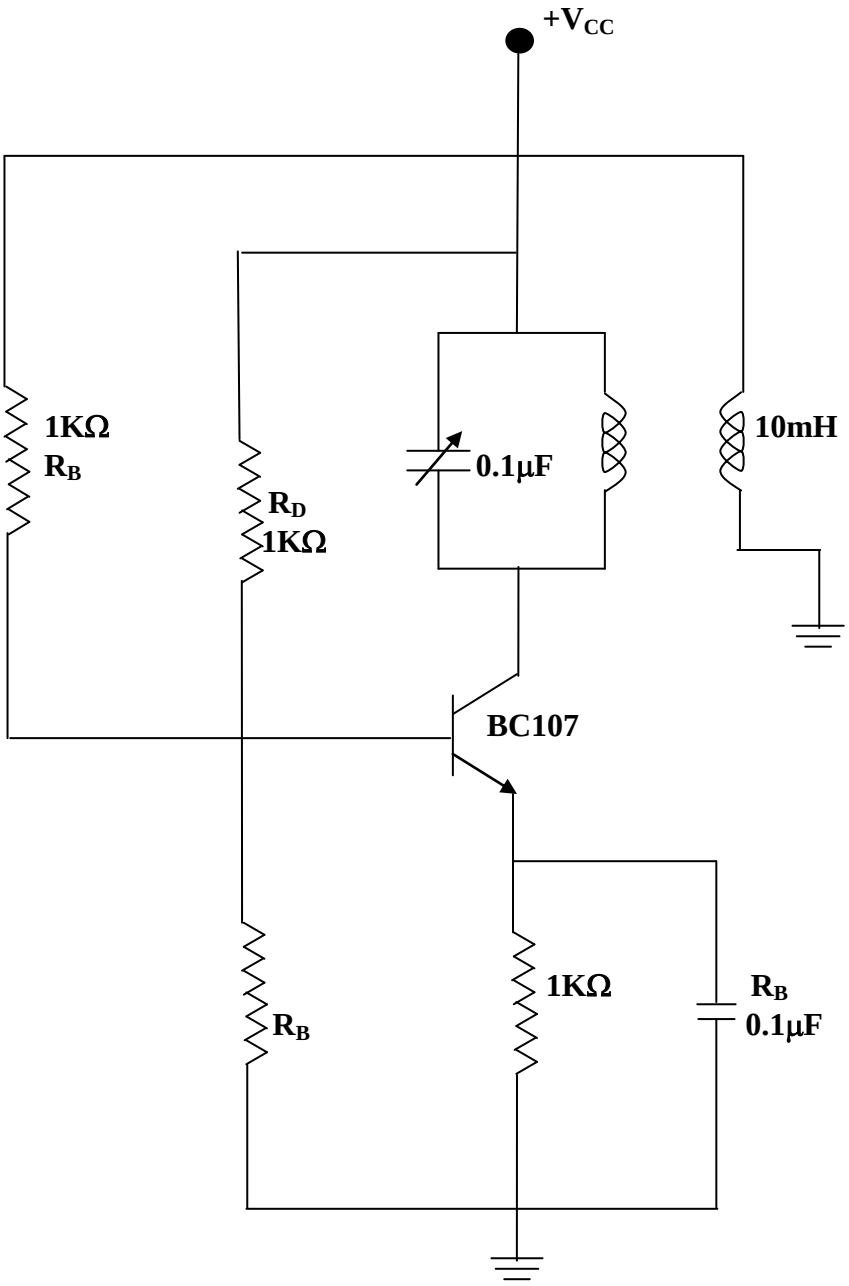
1. Wire the R/2R ladder 4 bit DAC circuit on the bread board.
2. Select the approximate value of R and 2R.
3. Reference voltage V_R is set as 5V .
4. Find the output voltage Vo for different combinations of digital binary inputs from 0000 to 1111.
5. Compare the calculated values with observed values and plot DAC characteristics.

Result:

Thus, the design of R/2R ladder 4-bit D/A Converter using IC 741 were done successfully..

SIMULATION USING PSPICE

Tuned Collector Oscillator



Ex. No.: 1 **TUNED COLLECTOR OSCILLATOR**

Aim:

To simulate the Tuned Collector Oscillator using Pspice net list.

Apparatus Required:

PC with Pspice software.

Theory:

Tuned collector oscillation is a type of transistor LC oscillator where the tuned circuit (tank) consists of a transformer and a capacitor is connected in the collector circuit of the transistor. Tuned collector oscillator is of course the simplest and the basic type of LC oscillators. The tuned circuit connected at the collector circuit behaves like a purely resistive load at resonance and determines the oscillator frequency.The common applications of tuned collector oscillator are RF oscillator circuits, mixers, frequency demodulators, signal generators etc

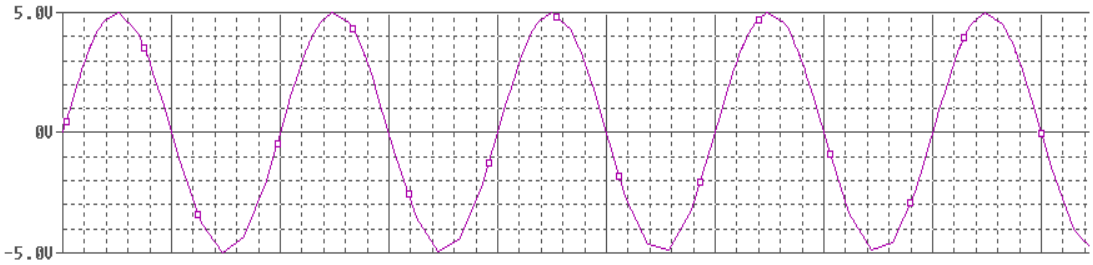
Procedure:

1. Open the text page of Pspice
2. Enter the coding program
3. Add the sub circuit file in text page, if need.
4. Save the coding with extension of circuit.
5. Open the saved circuits file and run the program.
6. Trace the output waveform.
7. Plot the output waveform.

Tuned Collector Oscillator

```
.lib nom.lib
vcc 4 0 dc 12v
rb 5 2 1k
r1 4 2 4.7k
r2 2 0 2k
re 1 0 1k
ce 1 0 0.1uf
c 3 4 0.1uf
L1 4 3 50mh
L2 5 0 10mh
K L1 L2 0.9999
q 3 2 1 BC107
.MODEL BC107 NPN
+ IS=10.000E-15
+ VAF=100
+ VAR=100
+ CJE=2.0000E-12
+ CJC=2.0000E-12
+ TF=10.000E-9
+ XTF=10
+ VTF=10
+ ITF=1
+ TR=10.000E-9
.tran 0 100us
.probe
.end
```

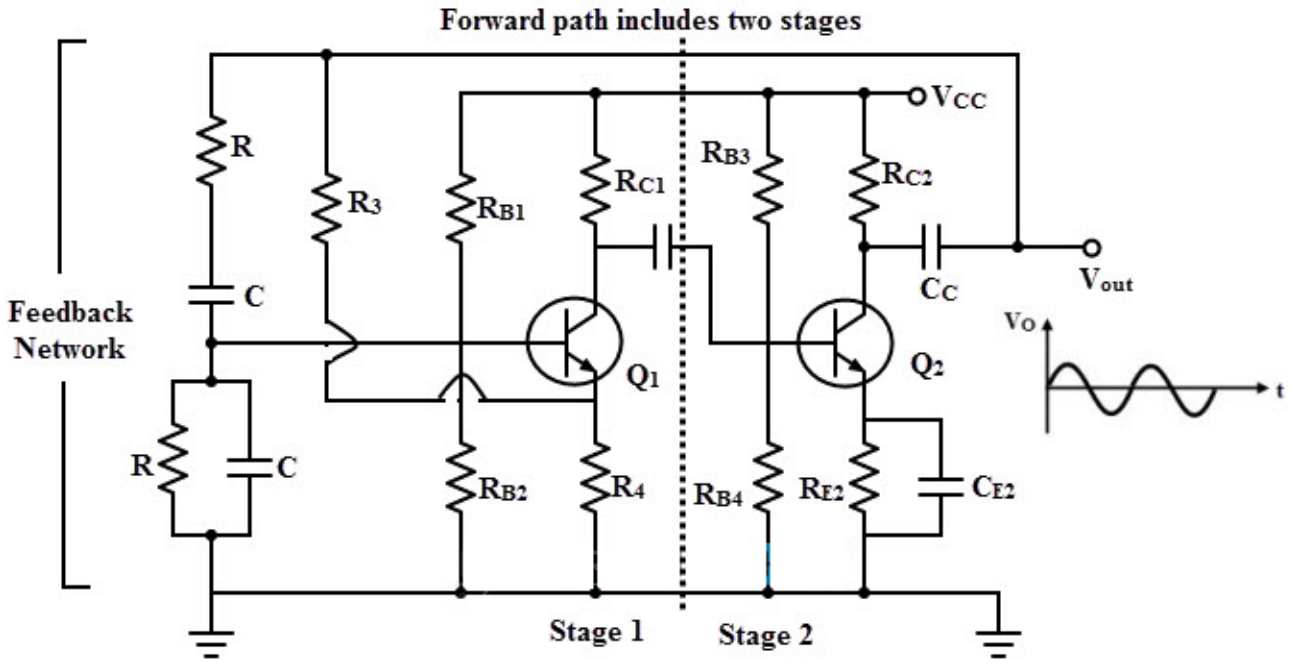
Output:



Result:

The performance of Tuned Collector Oscillator has been simulated and verified.

Wein Bridge Oscillator



Ex. No.: 2 **WIEN BRIDGE OSCILLATOR**

Aim:

To simulate the Wien Bridge Oscillator using Pspice net list.

Apparatus Required:

PC with Pspice software.

Theory:

Amplifier stage introduces 180°-phase shift and feedback network introduces 180° phase shift to obtain a phase shift of 360° around a loop. This is required condition for any oscillator. But Wein bridge oscillator uses a non-inverting amplifier and hence does not provide any phase shift during amplifier stage. As total phase shift is 0° in wein bridge type no phase shift is necessary through feedback. Total phase-shit around a loop is 0°

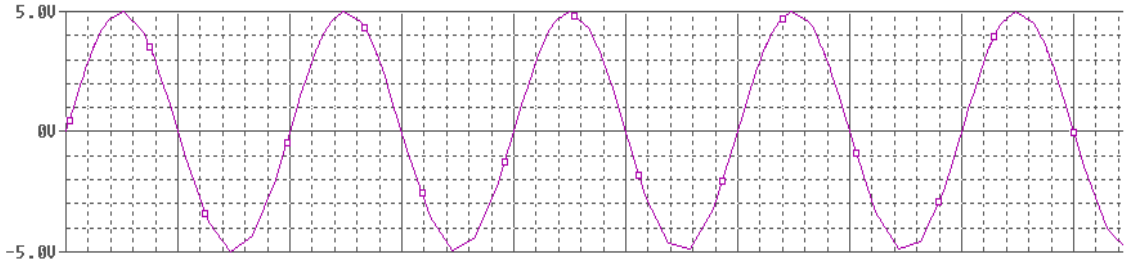
Procedure:

1. Open the text page of Pspice
2. Enter the coding program
3. Add the sub circuit file in text page, if need.
4. Save the coding with extension of circuit.
5. Open the saved circuits file and run the program.
6. Trace the output waveform.
7. Plot the output waveform.

Wein Bridge Oscillator

```
.lib nom.lib
vcc 10 0 dc 12v
r1 3 2 5.1k
r2 1 0 5.1k
c1 2 1 0.001uf
c2 1 0 0.001uf
r3 3 6 1k
rb1 10 5 10k
rb2 5 0 1k
rc1 10 4 1k
r4 6 0 220
cc1 4 8 .01uf
rb3 10 8 10k
rb4 8 0 1k
rc2 10 7 1k
re2 9 0 220
ce2 9 0 0.1uf
cc2 3 7 0.1uf
q1 4 5 6 BC107
q2 7 8 9 BC107
.MODEL bc107 NPN
+ IS=10.000E-15
+ VAF=100
+ VAR=100
+ CJE=2.0000E-12
+ CJC=2.0000E-12
+ TF=10.000E-9
+ XTF=10
+ VTF=10
+ ITF=1
+ TR=10.000E-9
.tran 0 100us
.probe
.end
```

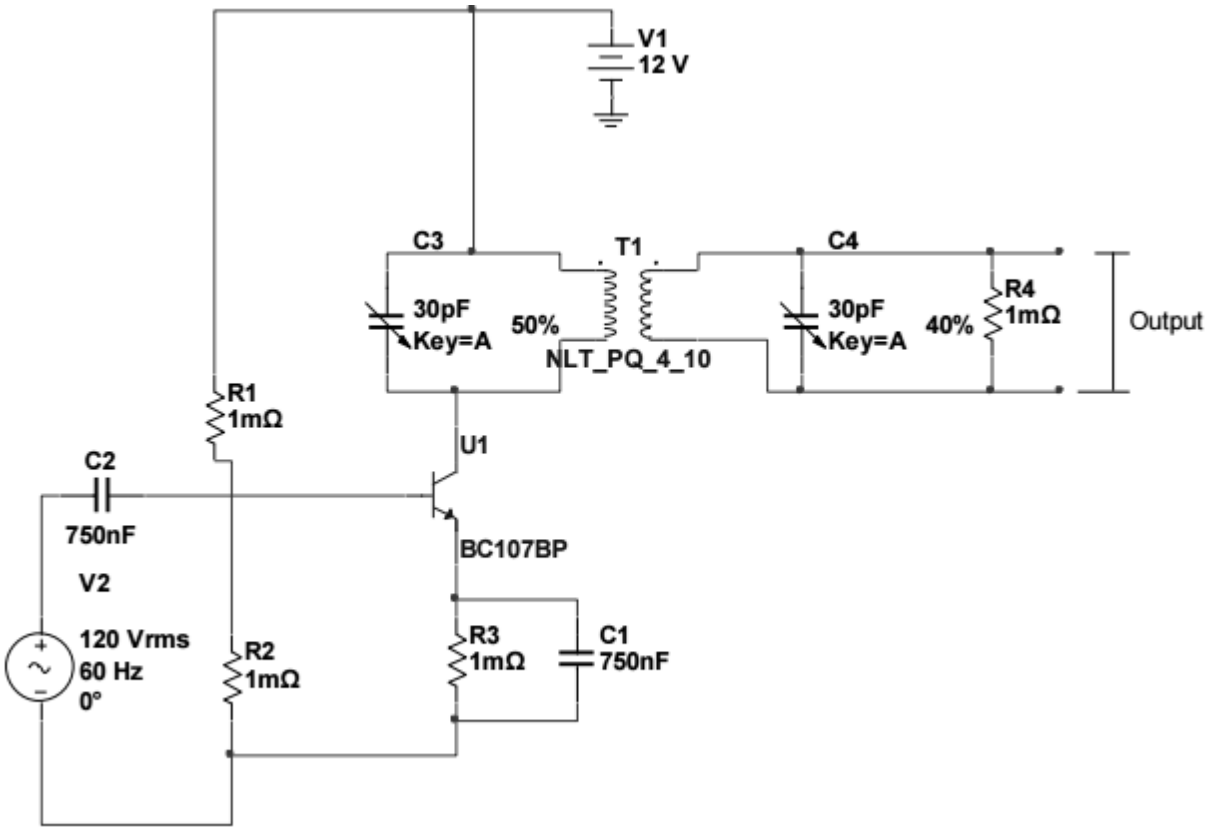
Output:



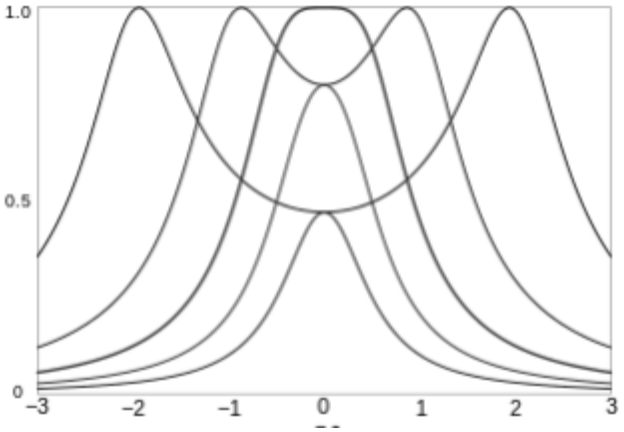
Result:

The performance of Wein Bridge Oscillator has been simulated and verified.

DOUBLE TUNED AMPLIFIER



Output:



Ex. No.: 3 (a) **DOUBLE TUNED AMPLIFIER**

Aim:

To simulate the Double and Stagger tuned Amplifiers using Pspice net list.

Apparatus Required:

PC with Pspice software.

Theory:

A double-tuned amplifier is a tuned amplifier with transformer coupling between the amplifier stages in which the inductances of both the primary and secondary windings are tuned separately with a capacitor across each. The scheme results in a wider bandwidth and steeper skirts than a single tuned circuit would achieve.

There is a critical value of transformer coupling coefficient at which the frequency response of the amplifier is maximally flat in the passband and the gain is maximum at the resonant frequency. Designs frequently use a coupling greater than this (over-coupling) in order to achieve an even wider bandwidth at the expense of a small loss of gain in the centre of the passband.

DOUBLE TUNED AMPLIFIER

```
.lib  nom . lib
Vcc  5  0  dc  12v
Vin  1  0  sin (0   5v 50KHz)
V1   5   2   1m
V2   2   0   1m
C1   3   0   750nf
C2   2   1   750nf
C3   5   4   30pf
C4   6   0   30pf
V3   3   0   1m
V4   6  0   1m
L1  5  4  50mb
L2  6  0  10mb
K  L1   L2  0.999
9 4  2  3  BC107
.MODEL BC107 NPN
+IS = 10.000E – 15
+VAF =100
+VAR =  100
+CJE  =  2.0000E – 12
+CJC = 2.0000 E- 12
+TF  =  10.  000 E – 9
+XTF = 10
+VTF = 10
+ITF = 1
+TR = 10.000E-9
.Tran  0  100ms
.Probe
.end
```

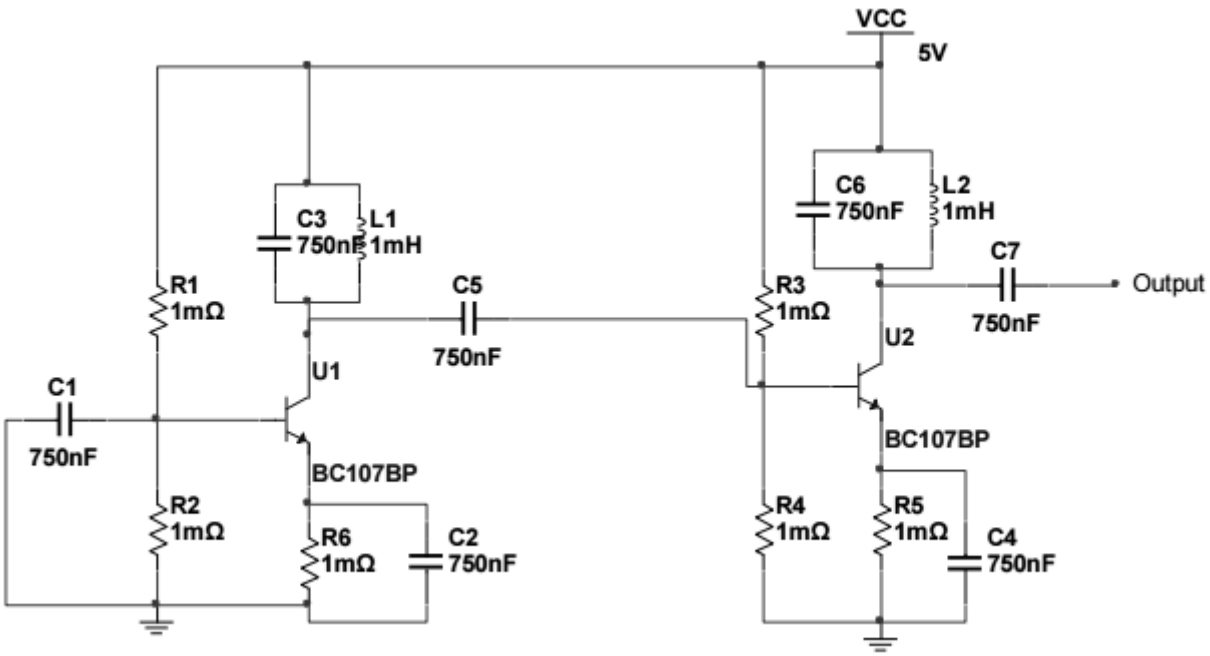
Procedure:

1. Open the text page of Pspice
2. Enter the coding program
3. Add the sub circuit file in text page, if need.
4. Save the coding with extension of circuit.
5. Open the saved circuits file and run the program.
6. Trace the output waveform.
7. Plot the output waveform.

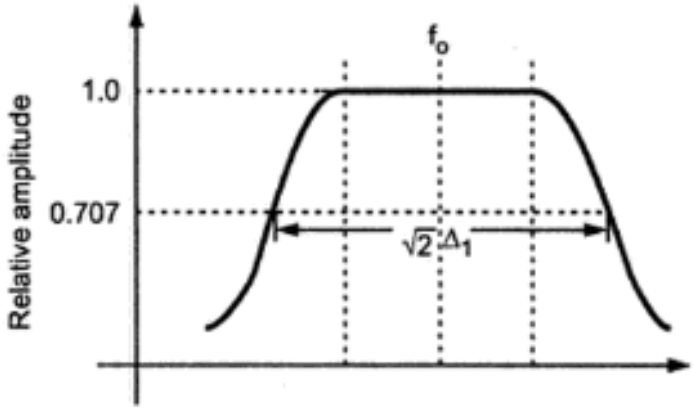
Result:

The performance of Double and Stagger tuned Amplifiers has been simulated and verified.

STAGGER TUNED AMPLIFIER



Output:



Ex. No.: 3 (b) **STAGGER TUNED AMPLIFIER**

Aim:

To simulate the Double and Stagger tuned Amplifiers using Pspice net list.

Apparatus Required:

PC with Pspice software.

Theory:

A double-tuned amplifier is a tuned amplifier with transformer coupling between the amplifier stages in which the inductances of both the primary and secondary windings are tuned separately with a capacitor across each. The scheme results in a wider bandwidth and steeper skirts than a single tuned circuit would achieve.

There is a critical value of transformer coupling coefficient at which the frequency response of the amplifier is maximally flat in the pass band and the gain is maximum at the resonant frequency. Designs frequently use a coupling greater than this (over-coupling) in order to achieve an even wider bandwidth at the expense of a small loss of gain in the centre of the pass band.

STAGGER TUNED AMPLIFIER

.lib nom. Lib

Vcc 4 0 dc 5v

V1 4 1 1m

V2 1 0 1m

V3 4 0 1m

V4 5 0 1m

V5 7 0 1m

V6 2 0 1m

Procedure:

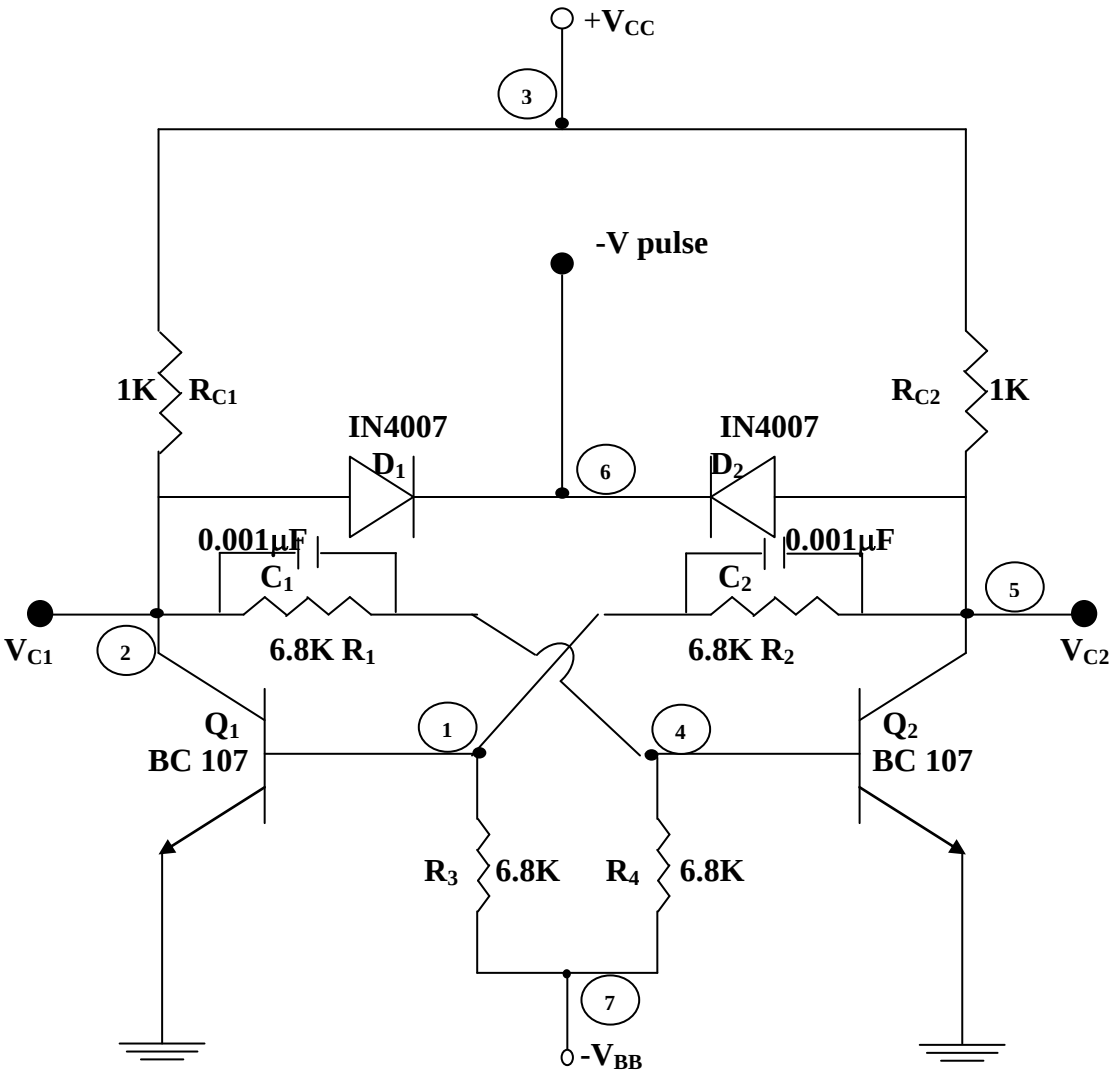
1. Open the text page of Pspice
2. Enter the coding program
3. Add the sub circuit file in text page, if need.
4. Save the coding with extension of circuit.
5. Open the saved circuits file and run the program.
6. Trace the output waveform.
7. Plot the output waveform.

Result:

The performance of Double and Stagger tuned Amplifiers has been simulated and verified.

BI-STABLE MULTIVIBRATOR

CIRCUIT DIAGRAM



Ex. No.: 4 **BISTABLE MULTIVIBRATORS**

Aim:

To simulate the Bistable Multivibrator using Pspice net list.

Apparatus Required:

PC with Pspice software.

Theory:

The bistable multivibrator is also referred to as flip-flop, Eccles-Jordan circuit, trigger circuit or binary. It has two stable states. A trigger pulse applied to the circuit will cause it to switch from one state to the other. Another trigger pulse is then required to switch the circuit back to its original state.

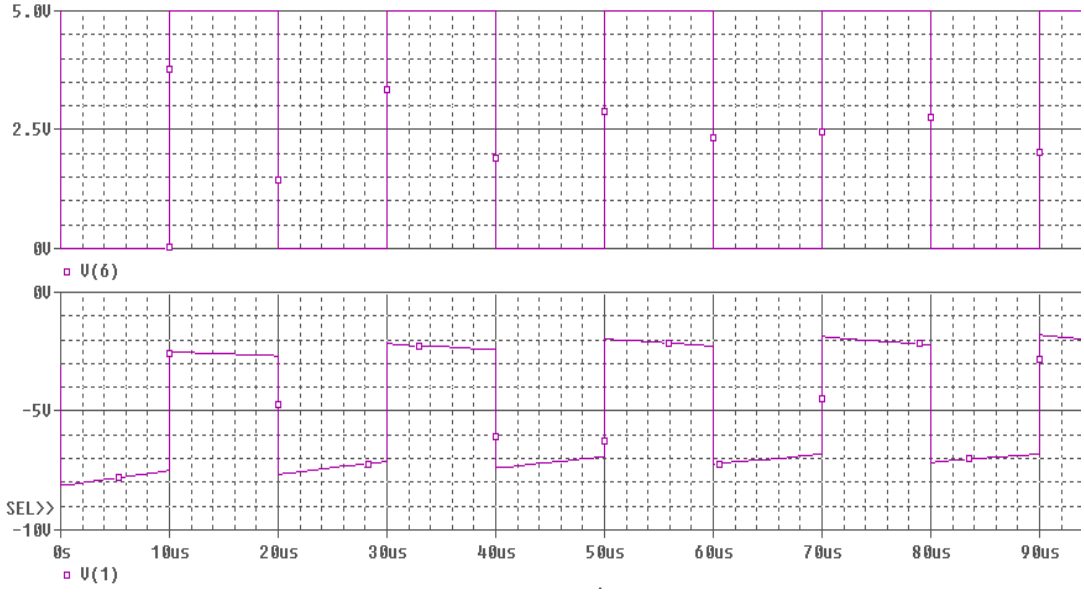
Procedure:

1. Open the text page of Pspice
2. Enter the coding program
3. Add the sub circuit file in text page, if need.
4. Save the coding with extension of circuit.
5. Open the saved circuits file and run the program.
6. Trace the output waveform.
7. Plot the output waveform.

Bistable Multivibrator

```
.lib nom.lib
vcc 3 0 dc 12v
vbb 0 7 dc 12v
v1 6 0 pulse (5v 0v 0 2ns 2ns 10us 20us)
rc1 3 2 1k
rc2 3 5 1k
r1 2 4 6.8k
r2 1 5 6.8k
r3 1 7 6.8k
r4 4 7 6.8k
c1 2 4 0.01uf
c2 1 5 0.01uf
d1 2 6 1N4007
d2 5 6 1N4007
* 1N4007 D model
* created using Model Editor release 9.1 on
03/19/15 at 09:44
* Model Editor is an OrCAD product.
.MODEL 1N4007 D
+ RS=1.0000E-3
+ CJO=1.0000E-12
+ M=.3333
+ VJ=.75
+ ISR=100.00E-12
+ BV=100
+ IBV=100.00E-6
+ TT=5.0000E-9
q1 2 1 0 BC107
q2 5 4 0 BC107
.MODEL BC107 NPN
+ IS=10.000E-15
+ VAF=100
+ VAR=100
+ CJE=2.0000E-12
+ CJC=2.0000E-12
+ TF=10.000E-9
+ XTF=10
+ VTF=10
+ ITF=1
+ TR=10.000E-9
.tran 0 100us
.probe
.end
```

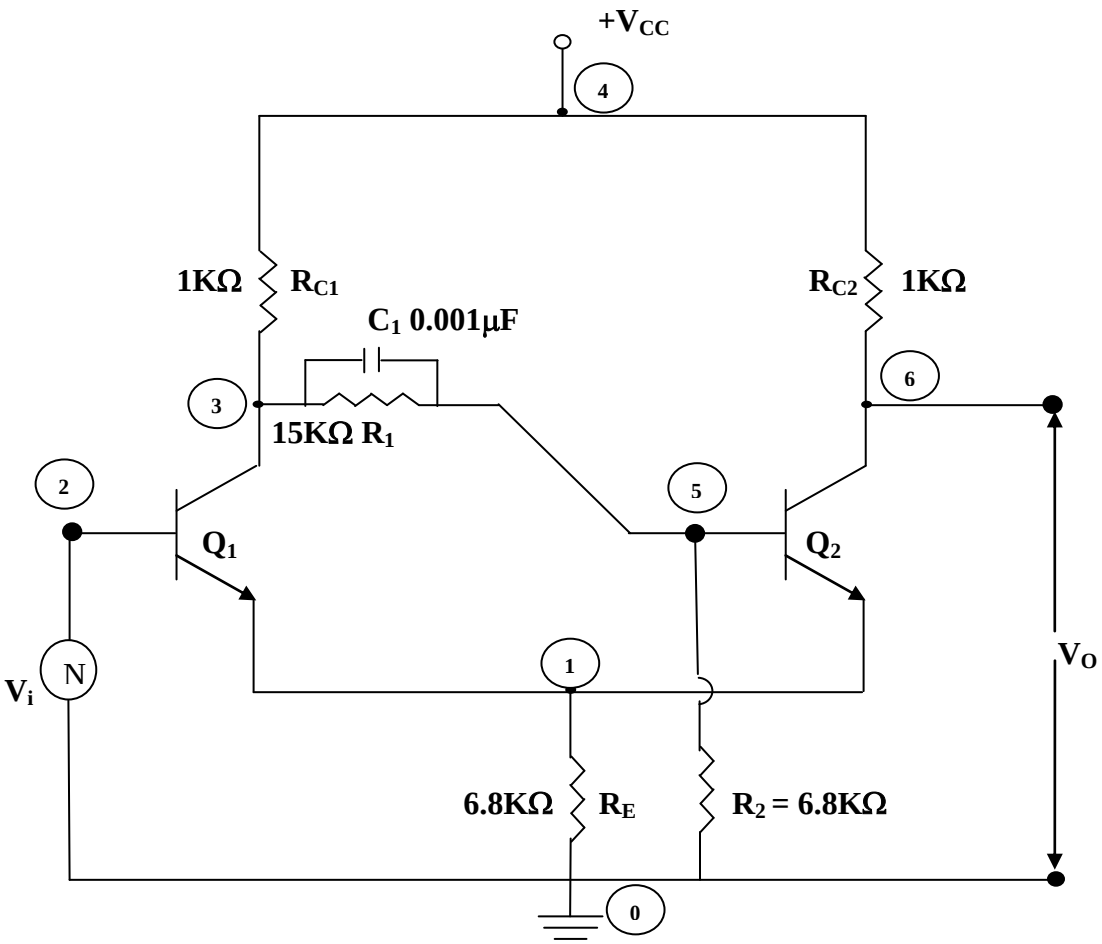
Output



Result:

The performance of Bistable Multivibrator has been simulated and verified.

Schmitt Trigger circuit with Predictable hysteresis



Ex. No.: 5 **SCHMITT TRIGGER CIRCUIT**

Aim:

To simulate the Schmitt Trigger circuit using Pspice net list.

Apparatus Required:

PC with Pspice software.

Theory:

It is also known as regenerative comparator, the input voltage is applied to the negative (-ve) input terminal and feedback voltage to the positive (+ve) input terminal. The input voltage V_i trigger the output V_O every time exceeds certain voltage levels are called upper threshold voltat3 (V_{UT}) and lower threshold voltage (V_{LT}). The hysteresis width is the difference between the two-threshold voltage ie. V_{UT}- V_{LT}- due to their hysteresis the circuit trigger at a higher voltage for increasing signals than for decreasing ones

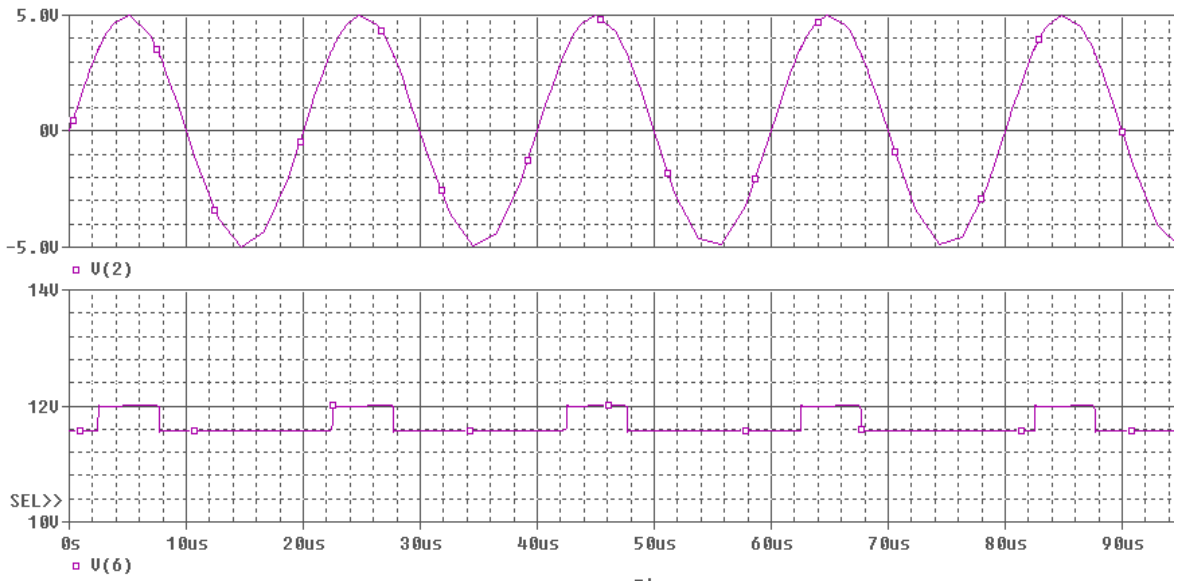
Procedure:

1. Open the text page of Pspice
2. Enter the coding program
3. Add the sub circuit file in text page, if need.
4. Save the coding with extension of circuit.
5. Open the saved circuits file and run the program.
6. Trace the output waveform.
7. Plot the output waveform.

Schmitt Trigger circuit with Predictable hysteresis

```
.lib nom.lib
vcc 4 0 dc 12v
vin 2 0 sin(0 5v 50khz)
rc1 4 3 1k
rc2 4 6 1k
r1 3 5 15k
re 1 0 6.8k
r2 5 0 6.8k
c 3 5 0.01uf
q1 3 2 1 BC107
q2 6 5 1 BC107
.MODEL BC107 NPN
+ IS=10.000E-15
+ VAF=100
+ VAR=100
+ CJE=2.0000E-12
+ CJC=2.0000E-12
+ TF=10.000E-9
+ XTF=10
+ VTF=10
+ ITF=1
+ TR=10.000E-9
.tran 0 100us
.probe
.end
```

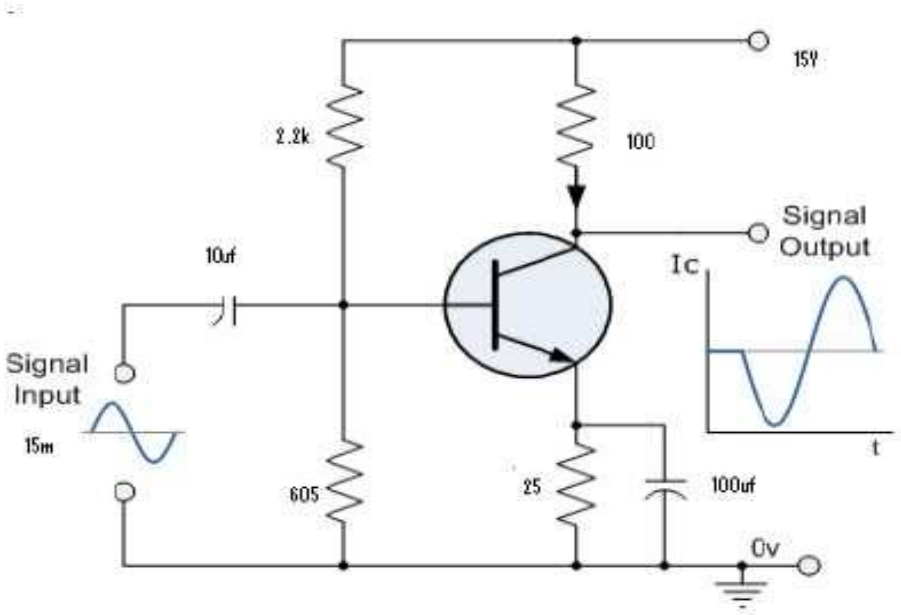
Output:



Result:

The performance of Schmitt Trigger circuit has been simulated and verified.

ANALYSIS OF POWER AMPLIFIER



Class C Power Amplifier:

. VS 1 0 SIN(0 5MV 10KHZ)
VCC 5 0 15V
CB 1 2 10UF
CC 3 6 10UF
CE 4 0 100UF
R1 5 2 2.7K
R2 2 0 605
RC 5 3 100
RE 4 0 25
RL 6 0 47
Q1 3 2 4 SL100
.MODEL SL100 NPN
.TRAN 0.1MS 0.5MS
.PROBE
.END

Ex. No.: 6 **ANALYSIS OF POWER AMPLIFIER**

Aim:

To analyze the characteristics of CLASS A Power Amplifier.

Apparatus Required:

PC with Pspice software.

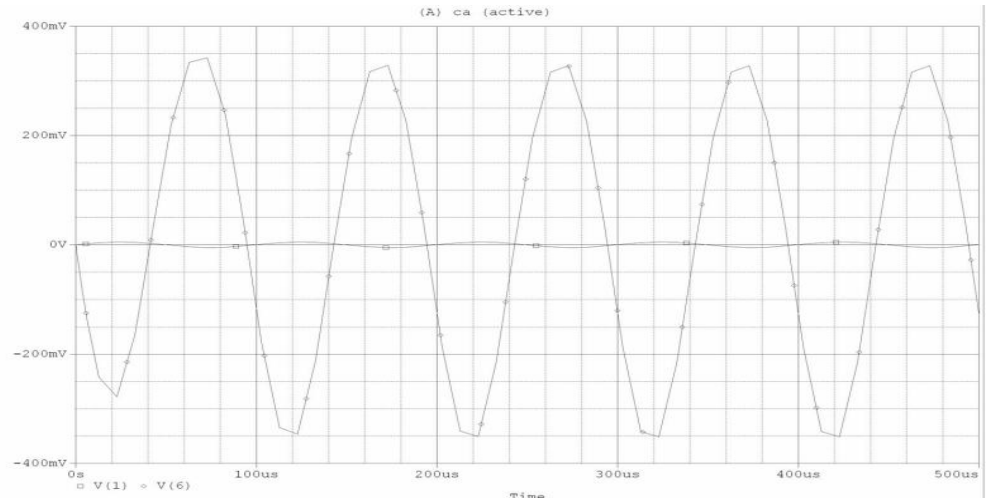
Theory:

An electronic amplifier is used for increasing the power of a signal. It does this by taking energy from a power supply and controlling the output to match the input signal shape but with a larger amplitude. In this sense, an amplifier may be considered as modulating the output of the power supply.

Procedure:

1. Open the text page of Pspice
2. Enter the coding program
3. Add the sub circuit file in text page, if need.
4. Save the coding with extension of circuit.
5. Open the saved circuits file and run the program.
6. Trace the output waveform.
7. Plot the output waveform.

Output:

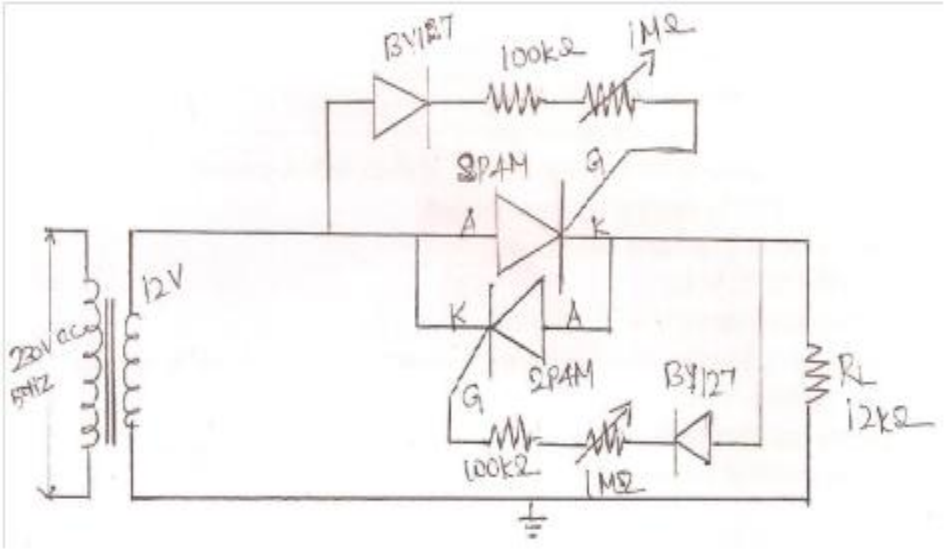


Result:

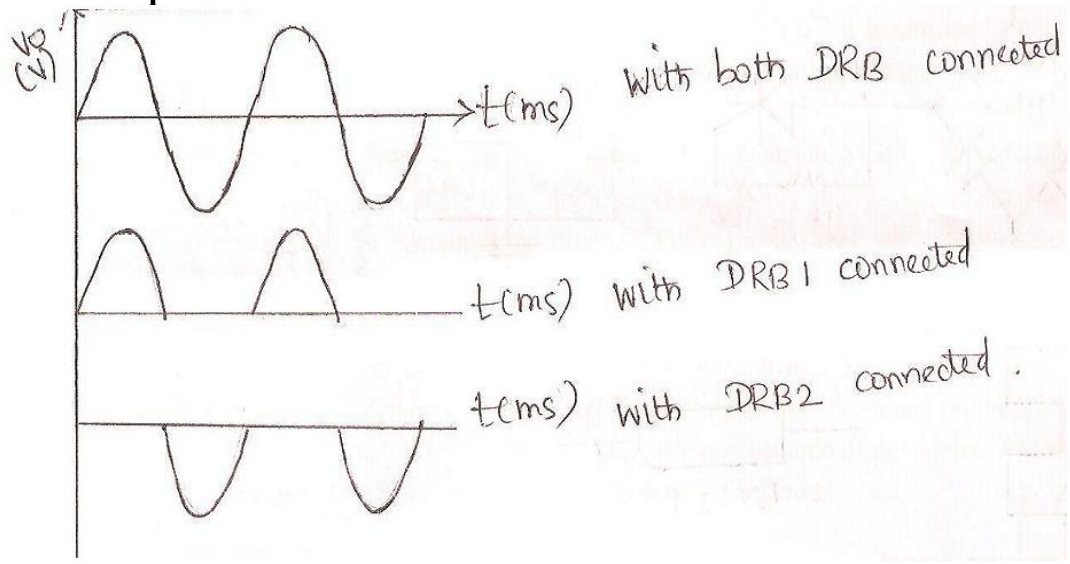
The characteristics of CLASS A Power Amplifier has been simulated and verified.

ADDITIONAL EXPERIMENTS
(BEYOND THE SYLLABUS)

Circuit diagram:



Model Graph:



Ex. No. : 1 **DESIGN OF AC VOLTAGE REGULATOR USING SCR**

AIM:

To design, construct and test a AC voltage regulator using SCR.

APPARATUS REQUIRED:

S.NO	Equipments & Components	Range	Quantity
1.	CRO	(0-30) MHz	1
2.	DRB		1
3.	Power Supply	(0-30) V	1
4.	Transformer	230V/12V	1
5.	Bread board		1
6.	Resistor	12K, 100KΩ.	Each 1
7.	Diode	BY 127	2
8.	SCR	2P4M	2
9.	Connecting wires		

Theory:

If the SCR is connected to AC supply and load, the power flow can be controlled by varying the RMS value of AC voltage applied to the load and this type of power circuit is caused as AC voltage regulator. Applications of AC voltage regulator are in heating on load transformers for changing light controls, speed controls and polyphase controls, induction motors and AC magnet controls for power transfer.

Two types of power control are normally used.

(1) ON-OFF control

(2) Polyphase Angle control

AC regulators are those converter which converts fixed ac voltage directly to variable ac voltage of the same frequency. The load voltage is regulated by controlling the firing angle of SCRs. AC voltage controllers are thyristor based devices.

The most common circuit is the inverse parallel SCR pair in which two isolated gate signals are applied. Each of the two SCRs are triggered at alternate half cycles of the supply and the load voltage is part of input sine wave. The SCR is an unidirectional device like diode, it allows current flow in only one direction but unlike diode, it has built-in feature to switch ON and OFF. The switching of SCR is controlled by gate and biasing condition. This switching property of SCR allows to control the ON periods thus controlling average power delivered to the load.

Tabular Column:

DRB 1 value(KΩ)	Amplitude (V)	T_{ON}(ms)
DRB 2 value(KΩ)	Amplitude (V)	T_{OFF}(ms)

Procedure:

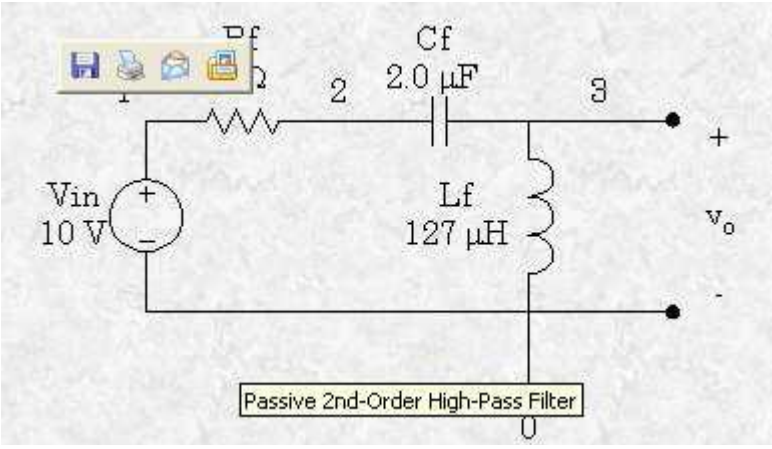
1. Connect the circuit as per the circuit diagram.
2. Switch on the power supply.
3. Observe the waveform both at DRB1 and DRB2.
4. Plot the waveform.

Result:

The AC voltage regulator using SCR was designed and the output waveforms are studied.

HIGH-PASS FILTER

CIRCUIT DIAGRAM



PROGRAM:

SPICE FILE
Vin 1 0 AC 10V
Rf 1 2 4.0
CF 2 3 2.0uF
Lf 3 0 127uH
.AC DEC 20 100Hz 1MEG
.PROBE
.END

Ex. No.: 2 **HIGH-PASS FILTER (Using PSPICE)**

AIM:

To design a high oass filter using the tool PSPICE.

APPARATUS REQUIRED:

PC with Pspice software.

THEORY:

A simple circuit for you to dive into running SPICE simulations and plotting results.

Basically it has two roles: to **pass** the desired high frequency signals and **stop** the unwanted low frequency signals.

PROCEDURE:

1. Open the text page of pspice
2. Enter the coding program
3. Add the sub circuit file in text page, if need.
4. Save the coding with extension of circuit.
5. Open the saved circuits file and run the program.
6. Trace the output waveform.
7. Plot the output waveform.

Result:

The high pass filter was designed ant the outputs are simulated using Pspice software.